4–40. A 2N2221, A, transistor is to be operated at 75°C. What is its maximum-rated power dissipation at that temperature?

4–41. The β of a 2N2218, A, transistor is 40 at T = 25°C, V_{CE} = 10 V, and I_C = 3 mA. What typical value for β could be expected at

(a) T = −55°C, I_C = 5 mA, and V_{CE} = 10 V?

(b) T = 175°C, I_C = 80 mA, and V_{CE} = 10 V?

4–42. The β of a 2N2219, A, transistor is 140 at T = 175°C, V_{CE} = 10 V, and I_C = 80 mA. What typical value for β could be expected at

(a) T = 25°C, I_C = 3 mA, and V_{CE} = 10 V?

(b) T = −55°C, I_C = 5 mA, and V_{CE} = 10 V?

4–43. What is the manufacturer's rated maximum value for the current I in Figure 4–76 Assume that T = 25°C.

4–44. A certain circuit is designed so that it will operate satisfactorily at T = 25°C if the transistor has a β of at least 50 when I_C = 10 mA and V_{CE} = 10 V. Can the 2N2222, A series transistor be used for the application?

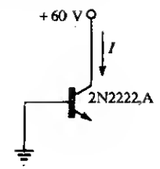


FIGURE 4–76 (Exercise 4–43)

SECTION 4–10

Transistor Curve Tracers

4–45. Using the curve tracer display of the collector characteristics shown in Figure 4–52(b), find the approximate β of the transistor when

(a) V_{CE} = 7 V and I_B = 8 μA, and

(b) V_{CE} = 8 V and I_B = 12 μA.

4–46. Using the curve tracer display of the diode characteristic shown in Figure 4–53, find the approximate dc resistance of the diode when it is forward biased by 0.64 V.

SPICE EXERCISES

Note: In the exercises that follow, assume all device parameters have their default values unless otherwise specified.

4–47. Use SPICE to obtain a set of output characteristics for an *npn* transistor in the CE configuration. The ideal maximum β is 150 and the Early voltage is 180 V. The characteristics should be plotted for V_{CE} ranging from 0 V to 12 V in 0.1 V steps and for I_B ranging from 0 to 50 μA in 10-μA steps.

4–48. Use SPICE to determine the bias point for the circuit shown in Figure 4–43 (Example 4–12). Set the ideal maximum forward β(BF) to 120 and then repeat the analysis with BF = 240. Comment on the effect the change in β has on the bias point. Use a silicon transistor.

4–49. Use SPICE to simulate the common-emitter circuit shown in Figure 4–37(a) (Example 4–10). Compare the change in the bias point when the temperature is changed from 27°C to 0°C.

4–50. Use SPICE to simulate a BJT inverter that is being driven by a 100-Hz TTL 5-V clock. Let the β of the transistor equal 100, R_C = 1 kΩ, R_S = 1 kΩ. Provide a plot of the output.

CHAPTER 5

FIELD-EFFECT TRANSISTORS

OUTLINE

OBJECTIVES

- Understand the basic operation of a JFET transistor
- Explore the basic dc bias configurations for the Junction Field Transistor
- Understand the modes of operation of the JFET transistor
- Apply the JFET transfer characteristic equation in circuit analysis
- Use the JFET transistor as an analog switch
- Understand the basic operation of the MOSFET transistor
- Use the JFET transistor in computer simulation

5–1 INTRODUCTION

The field-effect transistor (FET), like the bipolar junction transistor, is a three-terminal semiconductor device. However, the FET operates under principles completely different from those of the BJT. A field-effect transistor is called a *unipolar* device because the current through it results from the flow of only one of the two kinds of charge carriers: holes or electrons. The name *field effect* is derived from the fact that the current flow is controlled by an electric field set up in the device by an externally applied voltage.

There are two main types of FETs: the junction field-effect transistor (JFET) and the metal-oxide-semiconductor FET (MOSFET). We will study the theory and some practical applications of each. Both types are fabricated as discrete components and as components of integrated circuits. The MOSFET is the most important component in modern digital integrated circuits, such as microprocessors and computer memories.

5–2 JUNCTION FIELD-EFFECT TRANSISTORS

Figure 5–1 shows a diagram of the structure of a JFET and identifies the three terminals to which external electrical connections are made. As shown in the figure, a bar of *n*-type material has regions of *p* material embedded in each side. The two *p* regions are joined electrically, and the common connection between them is called the *gate* (G) terminal. A terminal at one end of the *n*-type bar is called the *drain* (D), and a terminal at the other end is called the *source* (S). The region of *n* material between the two opposing *p* regions is called the *channel*. The transistor shown in the figure is therefore called an *n-channel* JFET, the type that we will study initially, and a device constructed from a *p*-type bar with embedded *n* regions is called a *p-channel* JFET. As we develop the theory of the JFET, it may be helpful at first to think of the drain as corresponding to the collector of a BJT, the source as corresponding to the emitter, and the gate as corresponding to the base. As we shall see, the voltage applied to the gate controls the flow of current between drain and source, just as the signal applied to the base of a BJT controls the flow of current between collector and emitter.

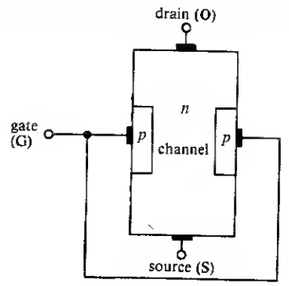


FIGURE 5–1 Structure of an *n*-channel JFET

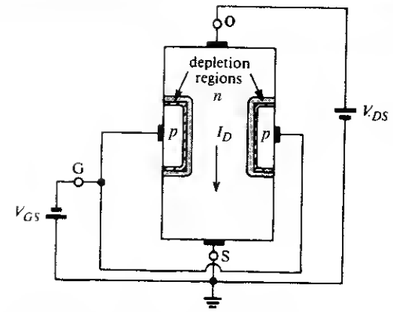
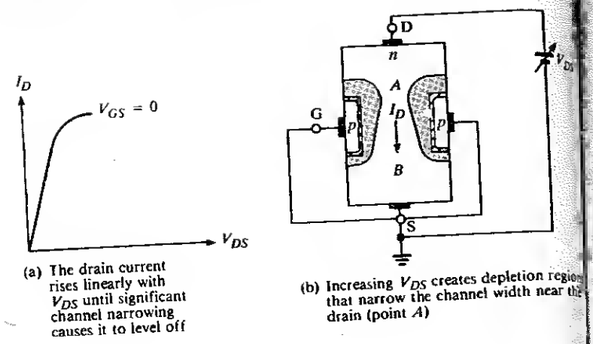


FIGURE 5–2 Reverse biasing the gate-to-source junctions causes the formation of depletion regions. V_{GS} is a small reverse-biasing voltage for the case illustrated.

When an external voltage is connected between the drain and the source of an *n*-channel JFET, so that the drain is positive with respect to the source, current is established by the flow of electrons through the *n* material from the source to the drain. (The source is so named because it is regarded as the origin of the electrons.) Thus, *conventional* current flows from drain to source and is limited by the resistance of the *n* material. In normal operation, an external voltage is applied between the gate and the source so that the *pn* junctions on each side of the channel are reverse biased. Thus, the gate is made negative with respect to the source, as illustrated in Figure 5–2. Note in the figure that the reverse bias causes a pair of depletion regions to form in the channel. The channel is more lightly doped than the gate, so the depletion regions penetrate more deeply into the *n*-type channel than into the *p* material of the gate.

The width of the depletion regions in Figure 5–2 depends on the magnitude of the reverse-biasing voltage V_{GS}. The figure illustrates the case where V_{GS} is only a few tenths of a volt, so the depletion regions are relatively narrow. (V_{DS} is also assumed to be relatively small; we will investigate the effect of a large V_{DS} presently.) As V_{GS} is made more negative, the depletion regions expand and the width of the channel decreases. The reduction in channel width increases the resistance of the channel and thus decreases the flow of current I_D from drain to source.

To investigate the effect of increasing V_{DS} on the drain current I_D, let us suppose for the moment that the gate is shorted to the source ($V_{GS} = 0$). As V_{DS} is increased slightly above 0, we find that the current I_D increases in direct proportion to it, as shown in Figure 5–3(a). This is as we would expect, because increasing the voltage across the fixed-resistance channel simply causes an Ohm's law increase in the current through it. As we continue to increase V_{DS}, we find that noticeable depletion regions begin to form in the channel, as illustrated in Figure 5–3(b). Note that the depletion regions are broader near the drain end of the channel (in the vicinity of point A) than they are near the source end (point B). This is explained by the fact that current flowing through the channel creates a voltage drop along the length of the channel. Near the top of the channel, the channel voltage is very nearly equal to V_{DS}, so there is a large reverse-biasing voltage between the *n* channel and the *p* gate. As we proceed down the channel, less voltage is available because of the drop that accumulates through the resistive *n* material. Consequently, the reverse-biasing potential between channel and gate



(a) The drain current rises linearly with V_{DS} until significant channel narrowing causes it to level off

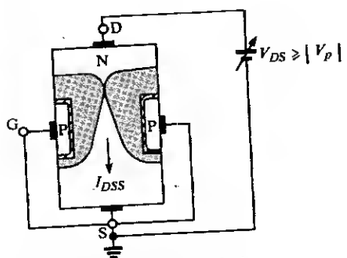
(b) Increasing V_{DS} creates depletion regions that narrow the channel width near the drain (point *A*)

FIGURE 5–3 Effects of increasing V_{DS} while the gate is shorted to the source ($V_{GS} = 0$)

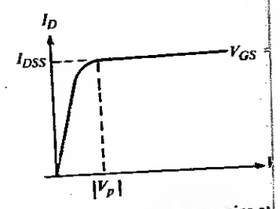
becomes smaller and the depletion regions become narrower as we approach the source. When V_{DS} is increased further, the depletion regions expand and the channel becomes very narrow in the vicinity of point A, causing the total resistance of the channel to increase. As a consequence, the rise in current is no longer directly proportional to V_{DS}. Instead, the current begins to level off as shown by the curved portion of the plot in Figure 5–3(a).

Figure 5–4(a) shows what happens when V_{DS} is increased to a value large enough to cause the depletion regions to meet at a point in the channel near the drain end. This condition is called *pinch-off*. At the point where pinch-off occurs, the gate-to-channel junction is reverse biased by the value of V_{DS}, so (the negative of) this value is called the *pinch-off voltage*, V_p. The pinch-off voltage is an important JFET parameter, whose value depends on the doping and geometry of the device. V_p is always a negative quantity for an *n*-channel JFET and a positive quantity for a *p*-channel JFET. Figure 5–4(b) shows that the current reaches a maximum value at pinch-off and that it remains at that value as V_{DS} is increased beyond $|V_p|$. This current is called the *saturation* current and is designated I_{DSS}—the Drain-to-Source current with the gate Shorted.

Despite the implication of the name *pinch-off*, note again that current continues to flow through the device when V_{DS} exceeds $|V_p|$. The value of the current remains constant at I_{DSS} because of a kind of self-regulating equilibrium process that controls the current when V_{DS} exceeds $|V_p|$: Suppose that an increase in V_{DS} *did* cause I_D to increase; then there would be in the channel an increased voltage drop that would expand the depletion regions further and reduce the current to its original value. Conversely, if current ceased to flow at pinch-off, the depletion region would shrink and current flow would resume. Of course, this change in current never actually occurs: I_D simply remains constant at I_{DSS}.



(a) When V_{DS} equals or exceeds the pinch-off voltage $|V_p|$, the depletion regions meet in the channel



(b) The drain current remains at saturation value I_{DSS} as V_{DS} increased beyond pinch-off

FIGURE 5–4 The *n*-channel JFET at pinch-off

FIGURE 5–5 Effects of increasing V_{DS} when $V_{GS} = -1$ V

A typical set of values for V_p and I_{DSS} are −4 V and 12 mA, respectively. Suppose we connect a JFET having those parameter values in the circuit shown in Figure 5–5(a). Note that the gate is no longer shorted to the source, but a voltage $V_{GS} = -1$ V is connected to reverse bias the gate-to-source junctions. The reverse bias causes the depletion regions to penetrate the channel farther along the entire length of the channel than they did when V_{GS} was 0. If we now begin to increase V_{DS} above 0, we find that the current I_D once more begins to increase linearly, as shown in Figure 5–5(b). Note that the slope of this line is not as steep as that of the $V_{GS} = 0$ line because the total resistance of the narrower channel is greater than before. As we continue to increase V_{DS}, we find that the depletion regions again approach each other in the vicinity of the drain. This further narrowing of the channel increases its resistance, and the current again begins to level off. Because there is already a 1–V reverse bias between the gate and the channel, the pinch-off condition, where the depletion regions meet, is now reached at $V_{DS} = 3$ V instead of 4 V ($V_{DS} = V_{GS} - V_p$). As shown in Figure 5–5(b), the current saturates at the lower value of 6.75 mA as V_{DS} is increased beyond 3 V.

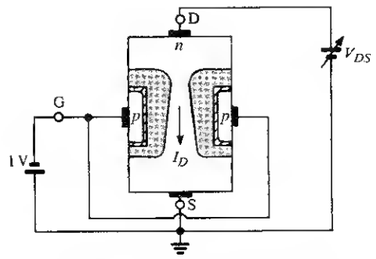
If the procedure we have just described is repeated with V_{GS} set to −2 V instead of −1 V, we find that pinch-off is reached at $V_{DS} = 2$ V and that the current saturates at $I_D = 3$ mA. It is clear that increasing the reverse-biasing value of V_{GS} (making V_{GS} more negative) causes the pinch-off condition to occur at smaller values of V_{DS} and that smaller saturation currents result. Figure 5–6 shows the family of characteristic curves, the *drain characteristics*, obtained when the procedure is performed for $V_{GS} = 0$, −1, −2, −3, and −4 V. The dashed line, which is parabolic, joins the points on each curve where pinch-off occurs. A value of V_{DS} on the parabola is called a *saturation voltage* $V_{DS(sat)}$. At any value of V_{GS}, the corresponding value of $V_{DS(sat)}$ is the difference between V_{GS} and V_p: $V_{DS(sat)} = V_{GS} - V_p$, as we have already described. The equation of the parabola is

$$I_D = I_{DSS}\left(\frac{V_{DS(sat)}}{V_p}\right)^2 \qquad (5\text{–}1)$$

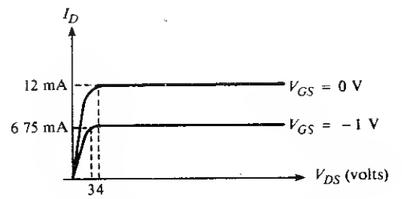
To illustrate, we have, in our example, $V_p = -4$ V and $I_{DSS} = 12$ mA, so at $V_{DS(sat)} = 3$ V we find

$$I_D = (12\text{ mA})\left(\frac{3}{-4}\right)^2 = 6.74\text{ mA}$$

which is the saturation current at the $V_{GS} = -1$ V line (see Figure 5–5(b)). Note in Figure 5–6 that the region to the right of the parabola is called the *pinch-off region*. This is the region in which the JFET is normally operated



(a) A reverse-biasing voltage $V_{GS} = -1$ V creates, along the length of the channel, a depletion region that is wider than when $V_{GS} = 0$ V



(b) As V_{DS} is increased, I_D increases linearly until pinch-off occurs at $V_{DS} = 3$ V

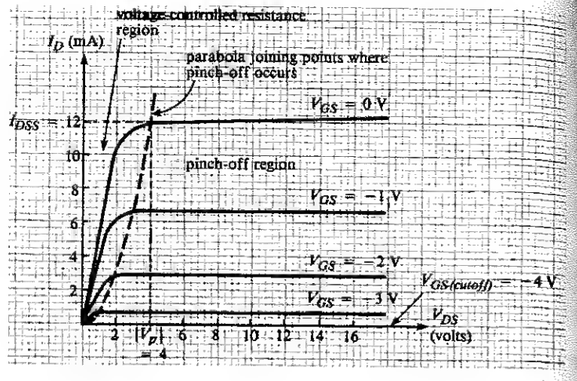


FIGURE 5–6 Drain characteristics of an *n*-channel JFET

when used for small-signal amplification. It is also called the *active* region, or the *saturation* region. The region to the left of the parabola is called the *voltage-controlled–resistance* region, the *ohmic* region, or the *triode* region. In this region, the resistance between drain and source is controlled by V_{GS}, as we have previously discussed, and we can see that the lines become less steep (implying larger resistance) as V_{GS} becomes more negative. The device acts like a voltage-controlled resistor in this region, and there are some practical applications that exploit this characteristic.

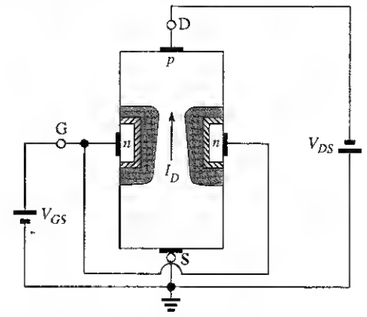
The line drawn along the horizontal axis in Figure 5–6 shows that $I_D = 0$ when $V_{GS} = -4$ V, regardless of the value of V_{DS}. When V_{GS} reverse biases the gate-to-source junction by an amount equal to V_p, depletion regions meet along the entire length of the channel and the drain current is cut off. Because the value of V_{GS} at which the drain current is cut off is the same as V_p, the pinch-off voltage is also called the *gate-to-source cutoff voltage*. Thus, there are two ways to determine the value of V_p from a set of drain characteristics: It is the value of V_{DS} where I_D saturates when $V_{GS} = 0$, and it is the value of V_{GS} that causes all drain current to cease, i.e., $V_p = V_{GS(cutoff)}$.

One property of a field-effect transistor that makes it especially valuable as a voltage amplifier is the very high input resistance at its gate. Because the path from gate to source is a reverse-biased *pn* junction, the only current that flows into the gate is the very small leakage current associated with a reverse-biased junction. Therefore, very little current is drawn from a signal source driving the gate, and the FET input looks like a very large resistance. A dc input resistance of several hundred megohms is not unusual. Although the gate of an *n*-channel JFET can be driven slightly positive, this action causes the input junction to be forward biased and radically decreases the gate-to-source resistance. In most practical applications, the sudden and dramatic decrease in resistance when the gate is made positive would not be tolerable to a signal source driving a FET.

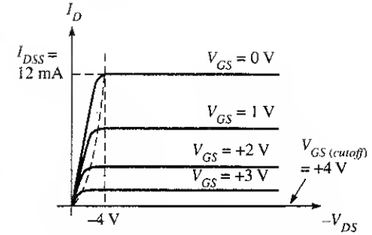
Figure 5–7 shows the structure and drain characteristics of a typical *p*-channel JFET. Since the channel is *p* material, current is due to hole flow, rather than electron flow, between drain and source. The gate material is, of course, *n*-type. Note that all voltage polarities are opposite those in the *n*-channel JFET. Figure 5–7(b) shows that positive values of V_{GS} control the amount of saturation current in the pinch-off region.

Figure 5–8 shows the schematic symbols used to represent *n*-channel and *p*-channel JFETs. Note that the arrowhead on the gate points into an

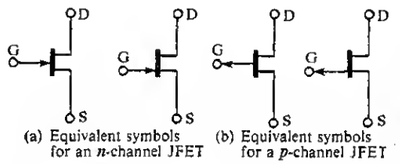
FIGURE 5–7 Structure and characteristics of a *p*-channel JFET



(a) The structure of a *p*-channel JFET



(b) Drain characteristics of a *p*-channel JFET. (Note that values of V_{DS} are negative and increase negatively to the right.)



(a) Equivalent symbols for an *n*-channel JFET (b) Equivalent symbols for a *p*-channel JFET

FIGURE 5–8 Schematic symbols for JFETs

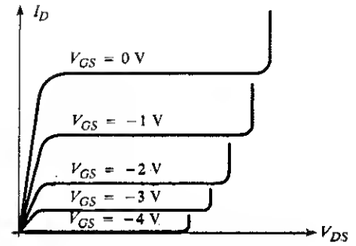


FIGURE 5–9 Breakdown characteristics of an *n*-channel JFET

n-channel JFET and outward for a *p*-channel device. The symbols showing the gate terminal off-center are used as a means of identifying the source: The source is the terminal drawn closest to the gate arrow. Some JFETs are manufactured so that the drain and source are interchangeable, and the symbols for these devices have the gate arrow drawn in the center.

Figure 5–9 shows the breakdown characteristics of an *n*-channel JFET. Breakdown occurs at large values of V_{DS} and is caused by the avalanche mechanism described in connection with BJTs. Note that the larger the magnitude of V_{GS}, the smaller the value of V_{DS} at which breakdown occurs.

Transfer Characteristics

The *transfer characteristic* of a JFET is a plot of output current versus input voltage, for a fixed value of output voltage. When the input to a JFET is the gate-to-source voltage and the output current is drain current (common-source configuration), the transfer characteristic can be derived from the drain characteristics. It is only necessary to construct a vertical line on the drain characteristics (a line of constant V_{DS}) and to note the value of I_D at each intersection of the line with a line of constant V_{GS}. The values of I_D can then be plotted against the values of V_{GS} to construct the transfer characteristic. Figure 5–10 illustrates the process.

In Figure 5–10, the transfer characteristic is shown for $V_{DS} = 8$ V. As can be seen in the figure, this choice of V_{DS} means that all points are in the pinch-off region. For example, the point of intersection of the $V_{DS} = 8$ V line and the $V_{GS} = 0$ V line occurs at $I_D = I_{DSS} = 12$ mA. At $V_{DS} = 8$ V and $V_{GS} = -1$ V, we find $I_D = 6.75$ mA. Plotting these combinations of I_D and V_{GS} produces the parabolic transfer characteristic shown. The nonlinear shape

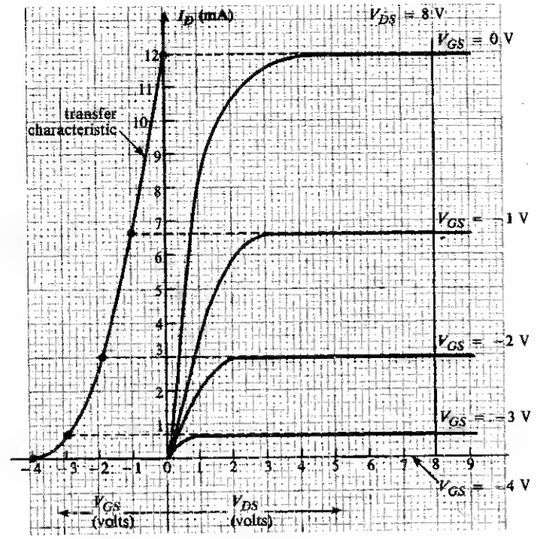


FIGURE 5–10 Construction of an *n*-channel transfer characteristic from the drain characteristics

of the transfer characteristic can be anticipated by observing that equal increments in the values of V_{GS} on the drain characteristics ($\Delta V_{GS} = 1$ V) do not produce equally spaced lines. (Recall from our discussion of BJT output characteristics that this situation creates output signal distortion when the device is used as an ac amplifier; practical JFET circuits incorporate a means for reducing distortion, at the expense of gain.) Note that the intercepts of the transfer characteristic are I_{DSS} on the I_D-axis and V_p on the V_{GS}-axis.

The equation for the transfer characteristic *in the pinch-off region* is, to a close approximation,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{5–2}$$

Note that equation 5–2 correctly predicts that $I_D = I_{DSS}$ when $V_{GS} = 0$ and that $I_D = 0$ when $V_{GS} = V_p$. The transfer characteristic is often called the *square-law* characteristic of a JFET and is used in some interesting applications to produce outputs that are nonlinear functions of inputs.

EXAMPLE 5–1

An n-channel JFET has a pinch-off voltage of −4.5 V and $I_{DSS} = 9$ mA.

1. At what value of V_{GS} in the pinch-off region will I_D equal 3 mA?
2. What is the value of $V_{DS(sat)}$ when $I_D = 3$ mA?

Solution

1. We must solve equation 5–2 for V_{GS}:

$$(1 - V_{GS}/V_p)^2 = I_D/I_{DSS}$$
$$1 - V_{GS}/V_p = \sqrt{I_D/I_{DSS}}$$
$$V_{GS} = V_p(1 - \sqrt{I_D/I_{DSS}})$$
$$V_{GS} = -4.5[1 - \sqrt{(3\text{ mA})/(9\text{ mA})}] = -1.9\text{ V}$$

2. Equation 5–1 relates I_D and $V_{DS(sat)}$. Solving for $V_{DS(sat)}$, we find

$$V_{DS(sat)} = \sqrt{(V_p)^2 I_D/I_{DSS}} = \sqrt{(4.5)^2(3\text{ mA})/(9\text{ mA})} = 2.6\text{ V}$$

Note that we use the positive square root, because V_{DS} is positive for an *n*-channel JFET. For a *p*-channel JFET, we would use the negative root. The value of $V_{DS(sat)}$ could also have been determined from the fact that $V_{DS(sat)} = V_{GS} - V_p = -1.9 - (-4.5) = 2.6$ V.

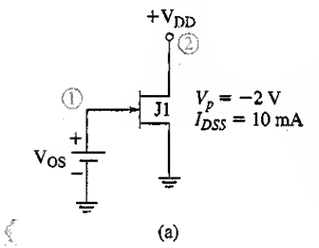
EXAMPLE 5–2

SPICE

Use SPICE to obtain a plot of the transfer characteristic of an *n*-channel JFET having $I_{DSS} = 10$ mA and $V_p = -2$ V. The characteristic should be plotted for $V_{DS} = 10$ V.

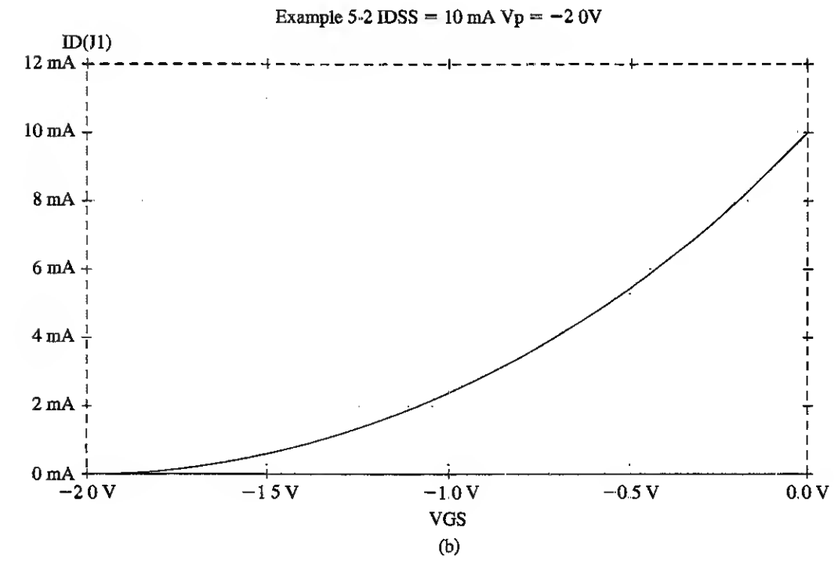
Solution

Figure 5–11(a) shows a SPICE circuit that can be used to obtain the desired characteristic. The value of BETA in the .MODEL statement is found from




```
EXAMPLE 5-2
VGS 1 0
J1 2 1 0 JFET
VDD 2 0 10V
.MODEL JFET NJF BETA=2.5E-3 VTO=-2
.DC VGS 0 -2 .1
.PROBE
.END
```

(a)



(b)

FIGURE 5–11 (Example 5–2)

$$\beta = \frac{I_{DSS}}{V_p^2} = \frac{10 \times 10^{-3}\ \text{A}}{(-2\ \text{V})^2} = 2.5 \times 10^{-3}\ \text{A/V}^2$$

Note that we step VGS from 0 to − 2 V in 0.1 V increments. The voltage source labeled VGS has its positive terminal connected to the gate of the FET, but the stepped voltages should all be negative. (Alternatively, we could reverse the polarity of VGS and step it through positive voltages.)

Figure 5–11(b) shows the plot produced by SPICE. (Rotate it 180° to obtain the orientation shown in Figure 5–10.) Note that $I_D = 10$ mA $= I_{DSS}$ when $V_{GS} = 0$ and that $I_D \approx 0$ when $V_{GS} = V_p$

5–3 JFET BIASING

Fixed Bias

Like a bipolar transistor, a JFET used as an ac amplifier must be biased in order to create a dc output voltage around which ac variations can occur. When a JFET is connected in the *common-source* configuration, the input voltage is V_{GS} and the output voltage is V_{DS}. Therefore, the bias circuit must set dc (quiescent) values for the drain-to-source voltage V_{DS} and drain current I_D. Figure 5–12 shows one method that can be used to bias *n*-channel and *p*-channel JFETs.

Notice in Figure 5–12 that a dc supply voltage V_{DD} is connected to supply drain current to the JFET through resistor R_D and that another dc voltage is used to set the gate-to-source voltage V_{GS}. This biasing method is called *fixed bias* because the gate-to-source voltage is fixed by the constant voltage applied across those terminals. Writing Kirchhoff's voltage law around the output loops in Figure 5–12, we find

$$\begin{aligned} V_{DS} &= V_{DD} - I_D R_D \quad (n\text{-channel}) \\ V_{DS} &= -V_{DD} + I_D R_D \quad (p\text{-channel}) \end{aligned} \tag{5–3}$$

When using these equations, always substitute a positive value for V_{DD} to ensure that the correct sign is obtained for V_{DS}. V_{DS} should always turn out to be a positive quantity in an *n*-channel JFET and a negative quantity in a *p*-channel JFET. For example, in an *n*-channel device where V_{DD} is +15 V from drain to ground, if $I_D = 10$ mA, and $R_D = 1$ kΩ, we have $V_{DS} = 15\ \text{V} - (10\ \text{mA})(1\ \text{k}\Omega) = +5\ \text{V}$. For a *p*-channel device where V_{DD} is −15 V from drain to ground, $V_{DS} = -15 + (10\ \text{mA}) \times (1\ \text{k}\Omega) = -5\ \text{V}$. Equations 5–3 can be rewritten in the form

$$\begin{aligned} I_D &= -(1/R_D)V_{DS} + V_{DD}/R_D \quad (n\text{-channel}) \\ I_D &= (1/R_D)V_{DS} + V_{DD}/R_D \quad (p\text{-channel}) \end{aligned} \tag{5–4}$$

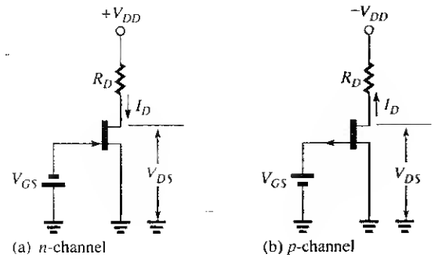


FIGURE 5–12 Fixed-bias circuits for *n*- and *p*-channel JFETs

Equations 5–4 are the equations of the dc load lines for *n*- and *p*-channel JFETs, and each can be plotted on a set of drain characteristics to determine a Q-point. This technique is the same as the one we used to determine the Q-point in a BJT bias circuit. The load line intersects the V_{DS}-axis at V_{DD} and the I_D-axis at V_{DD}/R_D.

EXAMPLE 5–3

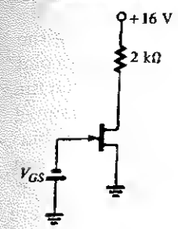


FIGURE 5–13 (Example 5–3)

The JFET in the circuit of Figure 5–13 has the drain characteristics shown in Figure 5–14. Find the quiescent values of I_D and V_{DS} when (1) $V_{GS} = -1.5$ V and (2) $V_{GS} = -0.5$ V.

Solution

1. The load line intersects the V_{DS}-axis at $V_{DD} = +16$ V and the I_D-axis at $I_D = (16\ \text{V})/(2\ \text{k}\Omega) = 8$ mA. It is plotted on Figure 5–14.
   At the intersection of the load line with $V_{GS} = -1.5$ V (labeled Q_1), we find the quiescent values $I_D \approx 4$ mA and $V_{DS} \approx 8$ V.
2. The load line is, of course, the same as in part (1). Changing V_{GS} to −0.5 V moves the Q-point to the point labeled Q_2 in Figure 5–14. Here we see that $I_D \approx 6.8$ mA and $V_{DS} \approx 2.4$ V.

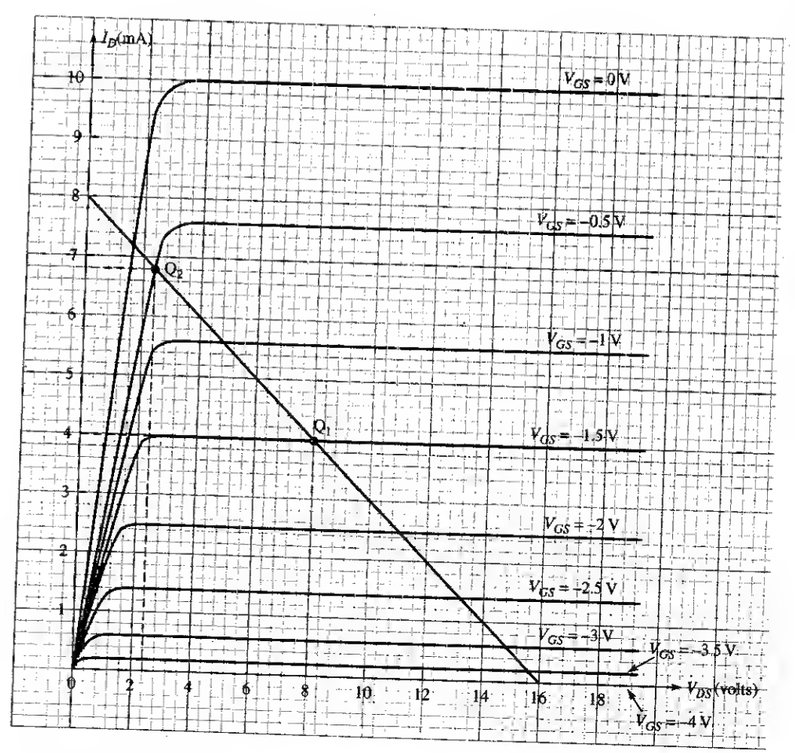


FIGURE 5–14 (Example 5–3)

Part 2 of the preceding example illustrates an important result. Note that changing V_{GS} to -0.5 V in the bias circuit of Figure 5–13 caused the Q-point to move out of the pinch-off region and into the voltage-controlled–resistance region. As we have already mentioned, the Q-point must be located in the pinch-off region for normal amplifier operation. *To ensure that the Q-point is in the pinch-off region, the quiescent value of* $|V_{DS}|$ *must be greater than* $|V_p| - |V_{GS}|$. The pinch-off voltage for the device whose characteristics are given in Figure 5–14 can be seen to be approximately -4 V. Because $|V_{GS}| = 0.5$ V and the quiescent value of V_{DS} at Q_2 is only 2.4 V, we do not satisfy the requirement $|V_{DS}| > |V_p| - |V_{GS}|$. Q_2 is therefore in the variable-resistance region.

Of course, the quiescent value of I_D can also be determined using the transfer characteristic of a JFET. Because the transfer characteristic is a plot of I_D versus V_{GS}, it is only necessary to locate the V_{GS} coordinate and read the corresponding value of I_D directly. The value of V_{DS} can then be determined using equation 5–3. Although graphical techniques for locating the bias point are instructive and provide insights into the way in which the circuit variables affect each other, the quiescent values of I_D and V_{DS} can be calculated using a straightforward computation, if the values of V_p and I_{DSS} are known. The next example illustrates that the square-law characteristic is used in this computation.

EXAMPLE 5–4

Given that the JFET in Figure 5–13 has $I_{DSS} = 10$ mA and $V_p = -4$ V, compute the quiescent values of I_D and V_{DS} when $V_{GS} = -1.5$ V. Assume that it is biased in the pinch-off region.

Solution

From equation 5–2,

$$I_D = I_{DSS}(1 - V_{GS}/V_p)^2 = (10\text{ mA})\left(1 - \frac{-1.5}{-4}\right)^2 = 3.9\text{ mA}$$

From equation 5–3, $V_{DS} = V_{DD} - I_D R_D = 16 - (3.9\text{ mA})(2\text{ k}\Omega) = 8.2$ V. These results are in close agreement with those obtained graphically in Example 5–3. Note that it was necessary to assume that the JFET is biased in the pinch-off region to justify the use of equation 5–2. If the computation had produced a value of V_{DS} less than $|V_p| - |V_{GS}| = 2.5$ V, we would have had to conclude that the device is not biased in pinch-off and would then have had to use another means to find the Q-point.

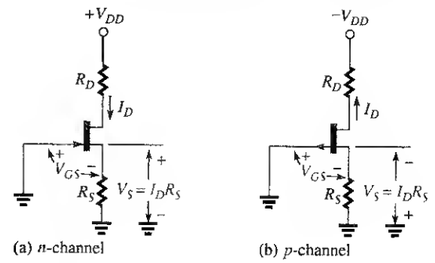
The values of I_{DSS} and V_p are likely to vary widely among JFETs of a given type. A variation of 50% is not unusual. When the fixed-bias circuit is used to set a Q-point, a change in the parameter values of the JFET for which the circuit was designed (caused, for example, by substitution of another JFET) can result in an intolerable shift in quiescent values. Suppose, for example, that a JFET having parameters $I_{DSS} = 13$ mA and $V_p = -4.3$ V is substituted into the bias circuit of Example 5–3 (Figure 5–13), with V_{GS} once again set to -1.5 V. Then

$$I_D = (13\text{ mA})\left(1 - \frac{-1.5}{-4.3}\right)^2 = 5.51\text{ mA}$$

$$V_{DS} = 16 - (5.51\text{ mA})(2\text{ k}\Omega) = 4.98\text{ V}$$

These results show that I_D increases 41.3% over the value obtained in Example 5–3 and that V_{DS} decreases 68.7%. Note also that the value of

FIGURE 5–15 Self-bias circuits



V_{DS} (4.98 V) is now perilously near the pinch-off voltage (4.3 V). We conclude that the fixed-bias circuit does not provide good Q-point stability against changes in JFET parameters.

Figure 5–15 shows a bias circuit that provides improved stability and requires only a single supply voltage. This bias method is called *self-bias* because the voltage drop across R_S due to the flow of quiescent current determines the quiescent value of V_{GS}. We can understand this fact by realizing that the current I_D in resistor R_S creates the voltage $V_S = I_D R_S$ at the source terminal, with respect to ground. For the *n*-channel JFET, this means that the source is positive with respect to the gate, because the gate is grounded. In other words, the gate is negative (by $I_D R_S$ volts) with respect to the source, as required for biasing an *n*-channel JFET: $V_{GS} = -I_D R_S$. For the *p*-channel device, the gate is positive by $I_D R_S$ volts, with respect to the source: $V_{GS} = I_D R_S$.

The equations

$$V_{GS} = -I_D R_S \quad (n\text{-channel}) \tag{5-5}$$

$$V_{GS} = I_D R_S \quad (p\text{-channel}) \tag{5-6}$$

describe straight lines when plotted on V_{GS}–I_D-axes. (Verify these equations by writing Kirchhoff's voltage law around each gate-to-source loop in Figure 5–15.) Each line is called the *bias line* for its respective type. The quiescent value of I_D in the self-bias circuit can be determined graphically by plotting the bias line on the same set of axes with the transfer characteristic. The intersection of the two locates the Q-point. In effect, we solve the bias-line equation and the square-law equation simultaneously by finding the point where their graphs intersect. The quiescent value of V_{DS} can be found by summing voltages (writing Kirchhoff's voltage law) around the output loops in Figure 5–15:

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \quad (n\text{-channel}) \\ V_{DS} &= -V_{DD} + I_D(R_D + R_S) \quad (p\text{-channel}) \end{aligned} \tag{5-7}$$

The next example illustrates the graphical procedure.

EXAMPLE 5–5

The transfer characteristic of the JFET in Figure 5–16 is given in Figure 5–17. Determine the quiescent values of I_D and V_{DS} graphically.

Solution

Because $R_S = 600\ \Omega$, the equation of the bias line is $V_{GS} = -600 I_D$. It is clear that the bias line always passes through the origin ($I_D = 0$ when $V_{GS} = 0$),

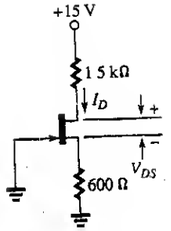
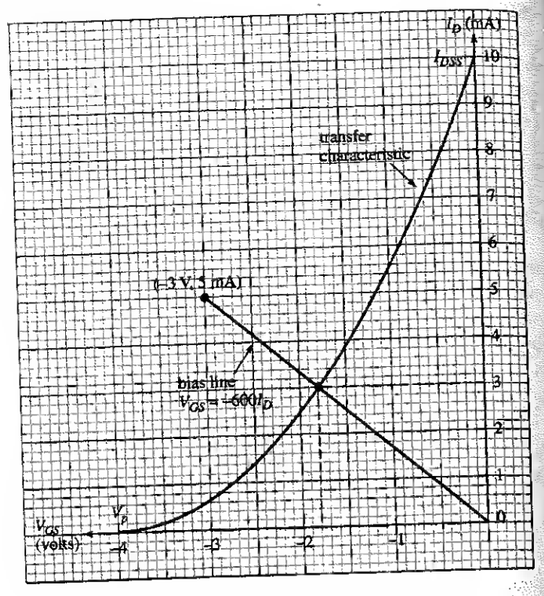


FIGURE 5–16
(Example 5–5)

FIGURE 5–17 (Example 6–5)



so (0,0) is one point on the line. To determine another point on the line, choose a convenient value of V_{GS} and solve for I_D. In this example, if we let $V_{GS} = -3$, then

$$I_D = \frac{-V_{GS}}{600\ \Omega} = \frac{-(-3\ \text{V})}{600\ \Omega} = 5\ \text{mA}$$

Thus, (−3 V, 5 mA) is another point on the bias line. We can then draw a straight line between the two points (0,0) and (−3 V, 5 mA) and note where that line intersects the transfer characteristic. The line is plotted on the transfer characteristic shown in Figure 5–17. We note that it intersects the characteristic at $I_D \approx 3$ mA, which is the quiescent drain current. The corresponding value of V_{GS} is seen to be approximately −1.8 V. The quiescent value of V_{DS} is found from equation 5–7.

$$V_{DS} = 15\ \text{V} - (3\ \text{mA})\,[(1.5\ \text{k}\Omega) + (0.6\ \text{k}\Omega)] = 8.7\ \text{V}$$

General Algebraic Solution—Self-Bias

The quiescent values of I_D and V_{GS} in the self-bias circuit can also be computed algebraically by solving the bias-line equation and the square-law equation simultaneously. To perform the computation, we must know the values of I_{DSS} and V_p. As in the fixed-bias case, the results are valid only if the Q-point is in the pinch-off region, i.e., if $|V_{DS}| > |V_p| - |V_{GS}|$. We must therefore assume that to be the case, but discard the results if the computation reveals the quiescent value of $|V_{DS}|$ to be less than $|V_p| - |V_{GS}|$. Equations 5–8 give the general form of the algebraic solution for the quiescent values of I_D, V_{DS}, and V_{GS} in the self-bias circuit. Because absolute values are used in the computations, the equations are valid for both *p*-channel and *n*-channel devices.

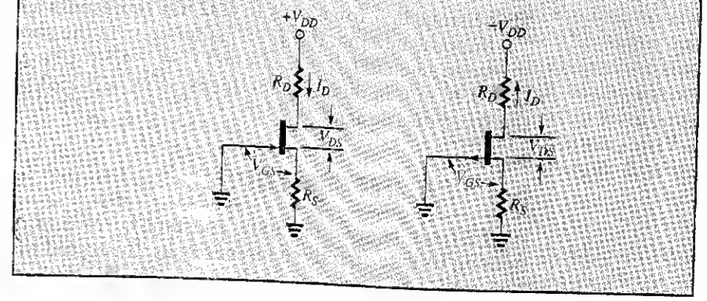
General algebraic solution for the bias point of self-biased JFET circuits

$$I_D = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \qquad (5\text{–}8)$$

where
$$A = R_S^2$$
$$B = -\left(2|V_p|R_S + \frac{V_p^2}{I_{DSS}}\right)$$
$$C = V_p^2$$
$$|V_{DS}| = |V_{DD}| - I_D(R_D + R_S) \quad \text{See note 1.}$$
$$|V_{GS}| = I_D R_S \quad \text{See note 2.}$$

Note 1. V_{DS} is positive for an *n*-channel JFET and negative for a *p*-channel JFET.

Note 2. V_{GS} is negative for an *n*-channel JFET and positive for a *p*-channel JFET.



EXAMPLE 5–6

Use equations 5–8 to find the bias point that was determined graphically in Example 5–5.

Solution

As shown in Figure 5–16, $R_S = 600\ \Omega$ and $R_D = 1.5\ \text{k}\Omega$. Also, the transfer characteristic in Figure 5–17 shows that $I_{DSS} = 10$ mA and $V_p = -4$ V. Thus, with reference to equations 5–8, we find

$$A = R_S^2 = (600)^2 = 3.6 \times 10^5$$
$$B = -\left(2|V_p|R_S + \frac{V_p^2}{I_{DSS}}\right) = -\left[2(4)(600) + \frac{(-4)^2}{10 \times 10^{-3}}\right] = -6.4 \times 10^3$$
$$C = V_p^2 = (-4)^2 = 16$$
$$I_D = \frac{-B - \sqrt{B^2 - 4AC}}{2A}$$
$$= \frac{6.4 \times 10^3 - \sqrt{40.96 \times 10^6 - 4(3.6 \times 10^5)(16)}}{2(3.6 \times 10^5)} = 3.0\ \text{mA}$$
$$|V_{DS}| = |V_{DD}| - I_D(R_D + R_S) = 15\ \text{V} - 3\ \text{mA}(1.5\ \text{k}\Omega + 600\ \Omega) = 8.7\ \text{V}$$
$$|V_{GS}| = I_D R_S = (3\ \text{mA})(600\ \Omega) = 1.8\ \text{V}$$

Because the JFET is *n*-channel, $V_{GS} = -1.8$ V. These results agree well with those found in Example 5–5. Because $|V_{DS}| = 8.7\text{ V} > |V_p| - |V_{GS}| = 4\text{ V} - 1.8\text{ V} = 2.2\text{ V}$, we know the bias point is in the pinch-off region and the results are valid.

To demonstrate that the self-bias method provides better stability than the fixed-bias method, let us compare the shift in the quiescent value of I_D that occurs using each method when the JFET parameters of the previous example are changed to $I_{DSS} = 12$ mA and $V_p = -4.5$ V. In each case, we will assume that the initial bias point (using a JFET with $I_{DSS} = 10$ mA and $V_p = -4$ V) is set so that $I_D = 3$ mA and that a JFET having the new parameters is then substituted in the circuit. We have already seen that $I_D = 3$ mA when $V_{GS} = -1.8$ V, so let us suppose that a fixed-bias circuit has V_{GS} set to -1.8 V. When I_{DSS} changes to 12 mA and V_p to -4.5 V, with V_{GS} fixed at -1.8 V, we find that the new value of I_D in the fixed-bias circuit is

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = (12 \times 10^{-3}\text{ A})\left(1 - \frac{1.8}{4.5}\right)^2 = 4.32\text{ mA}$$

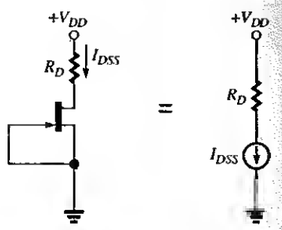
This change in I_D from 3 mA to 4.32 mA represents a 44% increase.

Suppose now that the JFET parameters in the self-bias circuit change by the same amount: $I_{DSS} = 12$ mA and $V_p = -4.5$ V. Using equations 5–8, we find $I_D = 3.46$ mA. In this case, the increase in I_D is 15.3%, less than half that of the fixed-bias design.

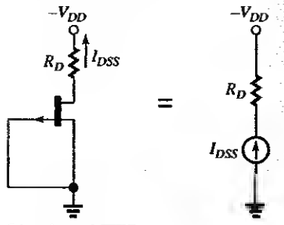
5–4 THE JFET CURRENT SOURCE

A JFET can be used to supply constant current to a variable load by connecting its gate directly to its source, as illustrated in Figure 5–18. Here, the resistor R_D is regarded as the (variable) load resistance. To be able to supply

FIGURE 5–18 JFET constant-current sources

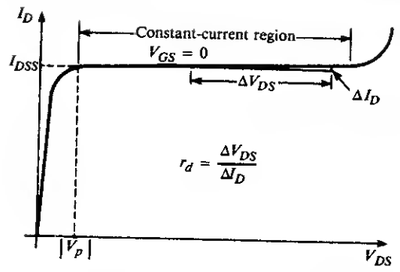


(a) *n*-channel JFET current source



(b) *p*-channel JFET current source

FIGURE 5–19 A JFET current source maintains an essentially constant current equal to I_{DSS} in the pinch-off region. If the characteristic were perfectly flat, then ΔI_D would equal zero and r_d would be infinite.



a current that is independent of R_D, the JFET must remain in its pinch-off region. Recall that the condition for pinch-off is $|V_{DS}| > |V_p| - |V_{GS}|$. Because $V_{GS} = 0$ in this case, the condition reduces to

$$|V_{DS}| > |V_p| \tag{5–9}$$

The constant current produced by the JFET is then $I_D = I_{DSS}$, because that is the drain current in the pinch-off region when $V_{GS} = 0$.

So long as the JFET is in its pinch-off region, the line corresponding to $V_{GS} = 0$ is essentially horizontal, meaning that the same current flows regardless of V_{DS}. See Figure 5–19. In reality, the line rises slightly to the right, so the current source is not perfect. Of course, no current source is perfect. The JFET current source would be perfect if r_d were infinite, which would be the case if the line were horizontal: $r_d = \Delta V_{DS}/\Delta I_D$ with $\Delta I_D = 0$. The JFET can also be used to supply a constant current equal to some value less than I_{DSS} by biasing it appropriately.

EXAMPLE 5–7

The JFET shown in Figure 5–20 has $V_p = -4$ V and $I_{DSS} = 14$ mA. What is the maximum value of R_L for which the circuit can be used as a constant-current source?

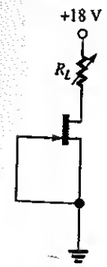


FIGURE 5–20 (Example 5–7)

Solution

To keep the JFET operating in the pinch-off region, we require

$$|V_{DS}| > |V_p|$$
$$18 - (14\text{ mA})R_L > 4$$
$$-14 \times 10^{-3}R_L > -14$$
$$R_L < \frac{14}{14 \times 10^{-3}} = 1\text{ k}\Omega$$

Thus, R_L must be less than 1 kΩ.

5–5 THE JFET AS AN ANALOG SWITCH

An *analog switch* is an electronically controlled device that will either pass or shut off a continuously varying analog-type signal. Figure 5–21 illustrates the concept. By way of contrast, a *digital switch* is one whose output switches between only two possible levels (low or high), such as the BJT inverter we discussed in Chapter 4. As illustrated in Figure 5–21, the analog switch is "opened" or "closed" by a digital-type input. Depending on the nature of the device, a high input may close the switch and a low input may open it, or vice versa. An analog switch is also called a *digital*

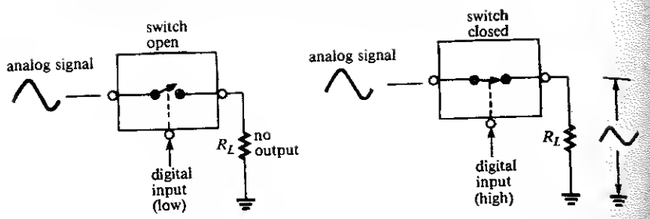


FIGURE 5–21 An analog switch connects or disconnects a variable (analog) signal, depending on the level of a digital input. In the arrangement shown, the switch is in series with the load R_L.

analog switch (DAS) because a digital input controls the switching of an analog signal.

A JFET can be used as an analog switch by connecting it as shown in Figure 5–22. Note that the analog signal (v_d) is connected to R_D, where a fixed supply voltage (V_{DD}) would normally be connected. The digital signal that opens and closes the switch is the gate-to-source voltage V_{GS}. V_{GS} is either 0 V, which causes the JFET to conduct, or V_p, a negative voltage (for an *n*-channel JFET) that cuts the JFET off. The output voltage of the switch, v_o, is the drain-to-source voltage, which will be either v_d (when the JFET is cut off) or close to 0 (when the JFET is conducting). Note that the switching arrangement is somewhat different from that shown in Figure 5–21 because the switch is now in *parallel* with the load resistance, R_L. When the switch is closed (JFET on), it effectively shorts out R_L; when the switch is open (JFET cut off), the short is removed.

When used as an analog switch, the JFET is operated in its voltage-controlled–resistance region rather than in pinch-off. As an aid in understanding how the JFET operates as a switch, refer to Figure 5–23, which shows a portion of the drain characteristics for $V_{GS} = 0$ and for $V_{GS} = V_p$. Only the rising portion of the $V_{GS} = 0$ curve in the voltage-controlled–resistance region is shown. The line corresponding to $V_{GS} = V_p$ coincides with the horizontal axis, because $I_D = 0$ in this case. Imagine that the variation in v_d creates a series of parallel load lines, each intersecting the V_{DS}-axis at an instantaneous value of v_d, just as a load line would intersect at V_{DD} if a fixed drain supply voltage were present. Thus, when $V_{GS} = V_p$, the values of V_{DS} are the same as the variations in v_d. This condition corresponds to that shown in Figure 5–22(c). When $V_{GS} = 0$, the operating point moves to the $V_{GS} = 0$ curve and the output voltage (V_{DS}) is very small. This corresponds to Figure 5–22(b). As long as V_{GS} remains at 0, the variations in I_D and V_{DS} are traced by a point that moves up and down the $V_{GS} = 0$

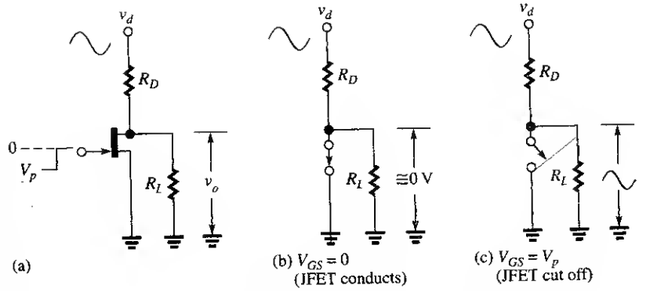


FIGURE 5–22 The JFET as an analog switch. Note that the switch is in parallel with R_L.

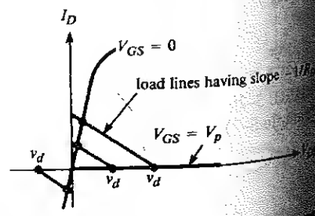


FIGURE 5–23 Operation of the JFET as an analog switch can be viewed as a variation in $V_{DS} = v_d$ along the horizontal axis (when $V_{GS} = V_p$) or as a variation along the $V_{GS} = 0$ curve when the JFET is conducting.

curve. For small variations, the curve is nearly linear and can be seen to be quite steep. The resistance ($\Delta V/\Delta I$) in this region is therefore very small and approximates the short-circuit condition we discussed for the case when the FET is "on" (conducting).

Note in Figure 5–23 that the $V_{GS} = 0$ curve extends into the third quadrant: the region where V_{DS} is negative and I_D is negative. This is the region of operation when the analog signal v_d goes negative and the current through the channel reverses direction. The reversal of polarity causes the gate-to-source junction to be forward biased but does not affect the *channel* resistance, so the slope of the $V_{GS} = 0$ curve is unchanged. The total variation in v_d must be small so that operation takes place over a small, nearly linear portion of the $V_{GS} = 0$ curve on either side of the origin. Also, R_D must be large enough to ensure that the variation occurs along the lower portion of the $V_{GS} = 0$ curve; that is, the load line should not be steep.

When the JFET is conducting, the small resistance $V_{DS}/I_D \approx v_{ds}/i_d$ in the region around the origin is called the *ON resistance*, $R_{D(ON)}$. Typical values range from 20 to 100 ohms. The smaller the value of $R_{D(ON)}$, the more nearly ideal the switch. Although a BJT switch has a lower ON resistance, the JFET switch has the advantage that $i_d = 0$ when $v_d = 0$.

EXAMPLE 5–8

The JFET in Figure 5–24 has $R_{D(ON)} = 50\ \Omega$. If $v_d = 100$ mV, what is the load voltage v_L (1) when $V_{GS} = V_p$ and (2) when $V_{GS} = 0$ V?

Solution

1. When $V_{GS} = V_p$, the JFET is cut off, and the circuit is equivalent to that shown in Figure 5–25. By the voltage-divider rule,

$$v_L = \left[\frac{100\ \text{k}\Omega}{(100\ \text{k}\Omega) + (10\ \text{k}\Omega)}\right](100\ \text{mV}) = 90.9\ \text{mV}$$

2. When $V_{GS} = 0$, the circuit is equivalent to that shown in Figure 5–26.

$$R_L \parallel R_{D(ON)} = (100\ \text{k}\Omega) \parallel (50\ \Omega) \approx 50\ \Omega$$

Therefore,

$$v_L = \left(\frac{50\ \Omega}{50\ \Omega + 10\ \text{k}\Omega}\right)(100\ \text{mV}) = 0.497\ \text{mV}$$

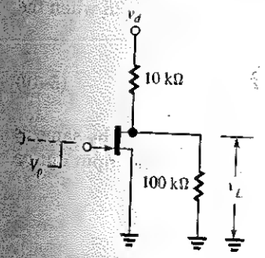


FIGURE 5–24 (Example 5–8)

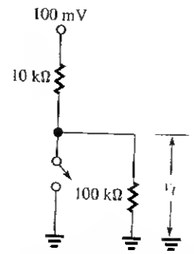


FIGURE 5–25 (Example 5–8) The circuit equivalent to Figure 5–24 when $V_{GS} = V_p$ and the JFET is cut off.

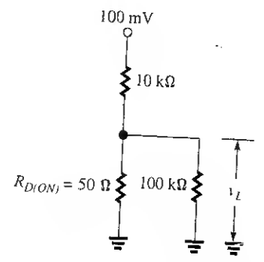


FIGURE 5–26 (Example 5–8) The circuit equivalent to Figure 5–24 when $V_{GS} = 0$ and the JFET is conducting.

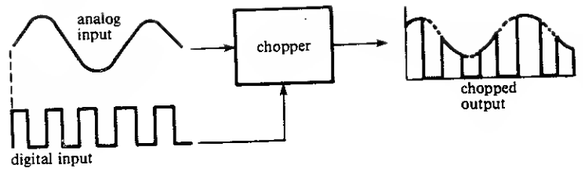


FIGURE 5–27 A chopper produces a series of pulses whose amplitudes follow the variations of an analog input signal

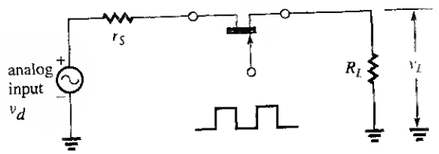


FIGURE 5–28 The JFET connected as a chopper Note that the switch is in series with the load

The JFET Chopper

A *chopper* is an analog switch that is turned on and off at a rapid rate by a periodic sequence of pulses, such as a square wave. It is used to convert a slowly varying signal into a series of pulses whose amplitudes vary slowly in the same way as the signal. Figure 5–27 illustrates the concept. A chopper is an example of a *modulator*—in this case, a pulse-amplitude modulator.

Figure 5–28 shows a JFET connected as a chopper. In this variation, the analog switch is in series with the load resistor, R_L, across which the chopped waveform is developed. When the switch is closed (JFET on), current flows from the analog signal source and into R_L. When the switch is open (JFET cut off), no current flows and the output voltage is 0.

Applying the voltage-divider rule to the circuit of Figure 5–28 when the JFET is on, we find

$$v_L = \left(\frac{R_L}{R_L + R_{D(ON)} + r_s}\right) v_d \qquad (5\text{–}10)$$

If R_L is much greater than $R_{D(ON)} + r_s$, then v_L is approximately the same as v_d. Thus, the amplitude of the output (pulse) follows the analog input during each interval when the JFET is conducting

5–6 MANUFACTURERS' DATA SHEETS

Figures 5–29 and 5–30 show typical data sheets for a series of *n*-channel JFETs: the 2N4220, 2N4221, and 2N4222. Note in particular the specification for the range of values of I_{DSS} for each device, as shown in Figure 5–29. We see, for example, that I_{DSS} for the 2N4222 can range from 5 mA to 15 mA. The pinch-off voltage (designated $V_{GS(off)}$) for the 2N4222 is seen to have a maximum value of −8 V. Devices having small values of I_{DSS} will have smaller values of $V_{GS(off)}$. Another important static characteristic shown in Figure 5–29 is I_{GSS}, the *gate reverse current,* which is the gate current when the gate–source junction is reverse biased, the normal mode of operation. This current provides a measure of the dc input resistance of the device, from gate to source. We see that the maximum specified value for the magnitude of I_{GSS} is 0.1 nA when $V_{GS} = -15$ V and $V_{DS} = 0$. Thus, the minimum gate-to-source resistance under those conditions is $R = (15\text{ V})/(0.1 \times 10^{-9}\text{ A}) = 150 \times 10^9\ \Omega$.

Figure 5–30 shows typical "performance curves" for the 2N4220 series of JFETs. The curves are also applicable to a number of similar JFETs

FIGURE 5–29 Manufacturer's specifications for a series of *n*-channel JFETs (Courtesy of Siliconix, Inc)

n-channel JFETs
designed for . . .

Siliconix

Performance Curves NRL
See Section 4

- **Small-Signal Amplifiers**
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

BENEFITS
- High Gain
- Low Receiver Noise Figure

2N4220 2N4220A 2N4221 2N4221A 2N4222 2N4222A

*ABSOLUTE MAXIMUM RATINGS (25°C)

TO-72
See Section 6

Gate Drain or Gate Source Voltage (Note 1)	-30 V
Gate Current	10 mA
Drain Current	15 mA
Total Device Dissipation at (or below) 25°C Free Air Temperature (Note 2)	300 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristics	2N4220, 2N4220A Min	2N4220, 2N4220A Max	2N4221, 2N4221A Min	2N4221, 2N4221A Max	2N4222, 2N4222A Min	2N4222, 2N4222A Max	Units	Test Conditions	
4	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
5				-0.1		-0.1		-0.1	μA		150°C
6	BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 μA, V_{DS} = 0	
7	$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		-8		V_{DS} = 15 V, I_D = 0.1 nA	
8	V_{GS}	Gate-Source Voltage	-0.5	-2.5	-1	-3	-2	-6	V		
			(0.5)	(5.0)	(2.0)	(6.0)	(5.0)	(15.0)	(μA)	V_{DS} = 15 V, I_D = 1	
9	I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	8	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
10	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000	4000	2000	5000	2800	6000			f = 1 kHz
11	y_{fs}	Common-Source Forward Transadmittance	780		750		750		μmho		f = 100 MHz
12	g_{os}	Common-Source Output Conductance (Note 3)		10		30		40		V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
13	C_{iss}	Common-Source Input Capacitance		6		6		6	pF		
14	C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			f = 1 MHz
15	NF	Noise Figure, Only 2N4220A, 2N4221A, 2N4222A		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg	f = 100 Hz

JEDEC registered data

NOTES

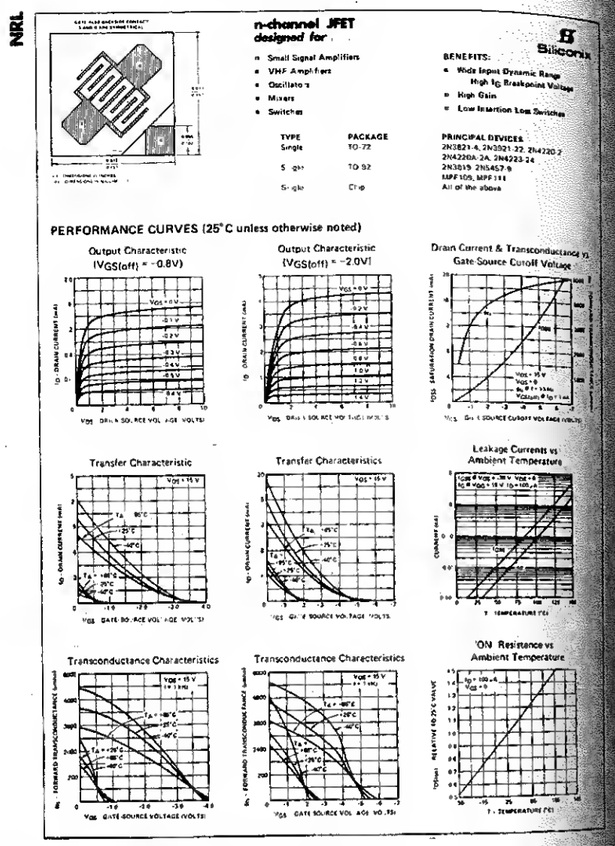
NRL

1. Due to commercial geometries these units may be operated with source and drain leads interchanged
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C
3. These parameters are measured during a 2 msec interval 100 msec after dc power is applied

produced by the manufacturer and show how wide a range of characteristics is possible. Note that two sets of output characteristics (drain characteristics) are shown, one representing a device having a small I_{DSS} (≈ 1.4 mA) and another having a larger I_{DSS} (≈ 4.2 mA).

Two sets of transfer characteristics are also shown in the figure These show the range that can be expected in the characteristic among devices of the same type, as well as variations due to temperature. The transfer characteristic in the center of the figure is applicable to the 2N4222 JFET. At 25°C, we see that any given 2N4222 could have a value V_p between about −2 V and −5 V. An interesting temperature phenomenon of JFETs is revealed by these characteristics. Note that the (maximum) value of I_{DSS} at 25°C is less than the value at −40°C, but greater than the value at 85°C. Although it is difficult to see in the figure, this result is accounted for by the fact that the three temperature curves intersect and cross through each other near the V_p end of the characteristics. For the 2N4222, this point can be seen to occur at about $V_{GS} = -4.5$ V. Thus, *the 2N4222 characteristics have zero temperature coefficient when the bias point is set at (about) −4.5 V.* For every JFET, there is a value of V_{GS} near V_p that results in a zero temperature coefficient.

FIGURE 5–30 Typical manufacturer's performance curves for *n*-channel JFETs (Courtesy of Siliconix, Inc.)



5–7 METAL-OXIDE-SEMICONDUCTOR FETS

The metal-oxide-semiconductor FET (MOSFET) is similar in many respects to its JFET counterpart, in that both have drain, gate, and source terminals and both are devices whose channel conductivity is controlled by a gate-to-source voltage. The principal feature that distinguishes a MOSFET from a JFET is the fact that the gate terminal in a MOSFET is *insulated* from its channel region. For this reason, a MOSFET is often called an *insulated-gate* FET, or IGFET.

Enhancement-Type MOSFETs

In the *n*-channel enhancement-type MOSFET, a *p*-type substrate extends all the way to an insulating SiO_2 layer adjacent to a metallic gate. This structure is shown in Figure 5–31.

Figure 5–32 shows the normal electrical connections between drain, gate, and source; the substrate is usually connected to the source. Notice that V_{GS} is connected so that *the gate is positive with respect to the source*. The positive gate voltage attracts electrons from the substrate to the region along the insulating layer opposite the gate. If the gate is made sufficiently positive, enough electrons will be drawn into that region to

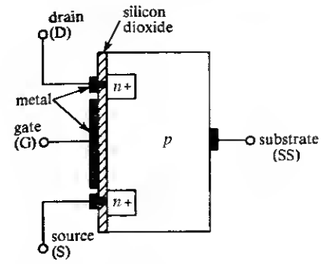


FIGURE 5–31 Enhancement-type MOSFET

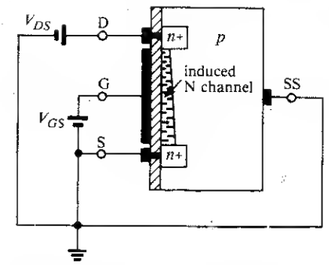
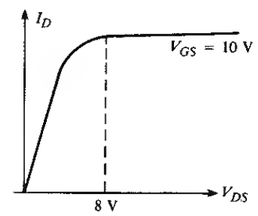


FIGURE 5–32 The positive V_{GS} induces an *n*-type channel in the substrate of an enhancement MOSFET

convert it to *n*-type material. Thus, an *n*-type channel will be formed between drain and source. The *p* material is said to have been *inverted* to form an *n*-type channel. If the gate is made still more positive, more electrons will be drawn into the region and the channel will widen, making it more conductive. In other words, making V_{GS} more positive *enhances* the conductivity of the channel and increases the flow of current from drain to source. Since electrons are induced into the channel to convert it to *n*-type material, the MOSFET shown in Figures 5–31 and 5–32 is often called an *induced n-channel* enhancement-type MOSFET. When this device is referred to simply as an *n*-channel enhancement MOSFET, it is understood that the *n* channel exists only when it is induced from the *p* substrate by a positive V_{GS}.

The induced *n* channel in Figure 5–32 does not become sufficiently conductive to allow drain current to flow until V_{GS} reaches a certain *threshold voltage*, V_T. In modern silicon MOSFETs, the value of V_T is typically in the range from 1 to 3 V. Suppose that $V_T = 2$ V and that V_{GS} is set to some value greater than V_T, say, 10 V. We will consider what happens when the drain-to-source voltage is gradually increased above 0 V. As V_{DS} increases, the drain current increases because of normal Ohm's law action. The current rises linearly with V_{DS}, as shown in Figure 5–33. As V_{DS} continues to increase, we find that the channel becomes narrower at the drain end, as illustrated in Figure 5–32. This narrowing occurs because the *gate-to-drain* voltage becomes smaller when V_{DS} becomes larger, thus reducing the positive field at the drain end. For example, if $V_{GS} = 10$ V and $V_{DS} = 3$ V, then $V_{GD} = 10 - 3 = 7$ V. When V_{DS} is increased to 4 V, $V_{GD} = 10 - 4 = 6$ V. The positive gate-to-drain voltage decreases by the same amount that V_{DS} increases, so the electric field at the drain end is reduced and the channel is narrowed. As a consequence, the resistance of the channel begins to increase, and the drain current begins to level off. This leveling off can be seen in the curve of Figure 5–33. When V_{DS}

FIGURE 5–33 The drain current in an *n*-channel enhancement MOSFET increases with V_{DS} until $V_{DS} = V_{GS} - V_T$ (= 10 − 2 = 8 V in this example)



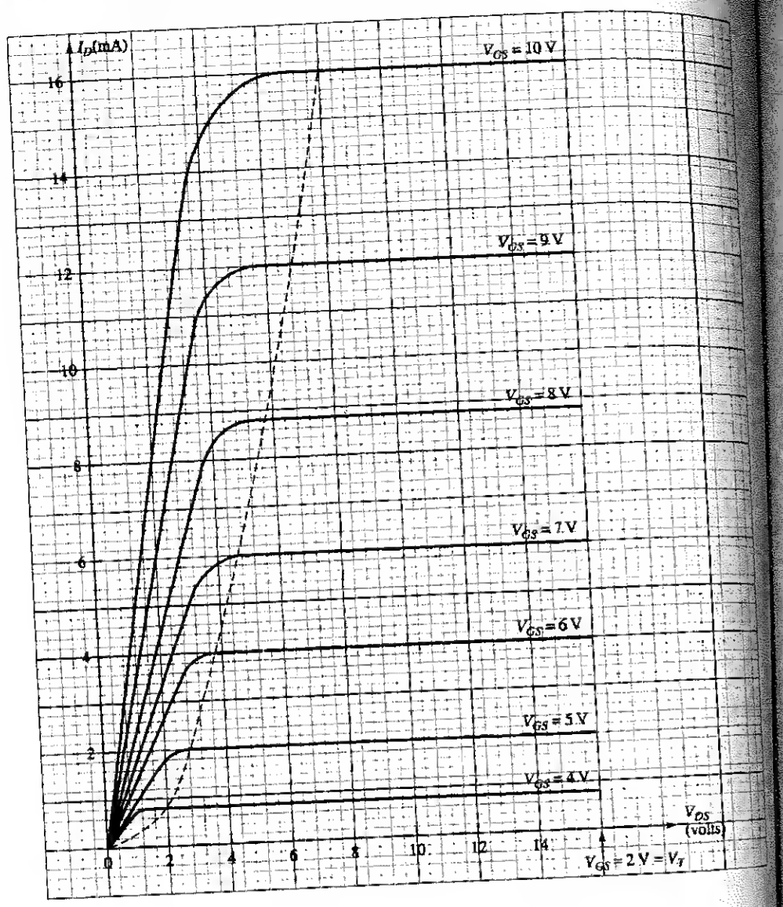


FIGURE 5–34 Drain characteristics of an induced *n*-channel enhancement MOSFET. Note that all values of V_{GS} are positive.

reaches 8 V, then $V_{GD} = 10 - 8 = 2\text{ V} = V_T$. That is, the positive voltage at the drain end reaches the threshold voltage, and the channel width at that end shrinks to zero. Further increases in V_{DS} do not change the shape of the channel, and the drain current does not increase any further; i.e., I_D saturates. This action is quite similar to the saturation that occurs at pinch-off in a junction FET.

When the process we have just described is repeated with V_{GS} fixed at 12 V, we find that saturation occurs at $V_{DS} = 12 - 2 = 10\text{ V}$. Letting $V_{DS(sat)}$ represent the voltage at which saturation occurs, we have, in the general case,

$$V_{DS(sat)} = V_{GS} - V_T \tag{5-11}$$

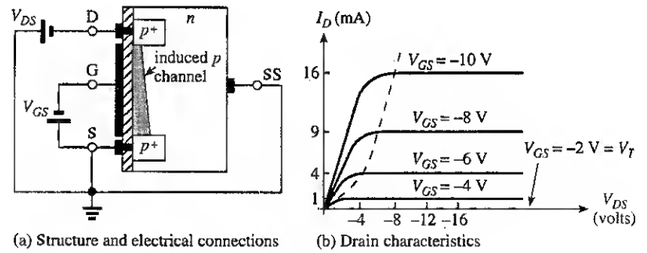
Figure 5–34 shows a set of drain characteristics resulting from repetitions of the process we have described, with V_{GS} set to different values of positive voltage. When V_{GS} is reduced to the threshold voltage $V_T = 2\text{ V}$, notice that I_D is reduced to 0 for all values of V_{DS}. The drain characteristics are similar to those of an *n*-channel JFET, except that all values of V_{GS} are pos-

itive in the case of the enhancement MOSFET. The enhancement MOSFET can be operated only in an enhancement mode, unlike the depletion MOSFET, which can be operated in both depletion and enhancement modes. The dashed, parabolic line shown on the characteristics in Figure 5–34 joins the saturation voltages, i.e., those satisfying equation 5–11. As in JFET characteristics, the region to the left of the parabola is called the *voltage-controlled–resistance* region where the drain-to-source resistance changes with V_{GS}. We will refer to the region to the right of the parabola as the *active region*. The device is normally operated in the active region for small-signal amplification.

Figure 5–35(a) shows the structure of a *p*-channel enhancement MOSFET and its electrical connections. Note that the substrate is *n*-type material and that a *p*-type channel is induced by a negative V_{GS}. The field produced by V_{GS} drives electrons away from the region near the insulating layer and inverts it to *p* material. Figure 5–35(b) shows a typical set of drain characteristics for the *p*-channel enhancement MOSFET. Note that all values of V_{GS} are negative and that the threshold voltage V_T is negative. *n*-channel and *p*-channel MOSFETs are often called *NMOS* and *PMOS* devices for short.

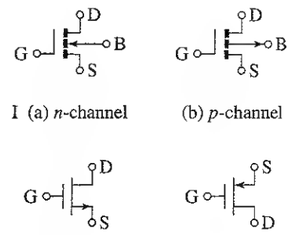
Figure 5–36 shows the schematic symbols typically used to represent *n*-channel and *p*-channel enhancement MOSFETs. Symbols I (a) and (b) are typically used when the bulk substrate (B) connection needs to be shown. The broken line symbolizes the fact that the channel is induced rather than being an inherent part of the structure. The broken-line symbol is not always used and is replaced with a solid line. Symbols II (a) and (b) are typically used when the source and bulk connections are shorted together, $V_{SB} = 0$. Both sets of symbols are commonly used when preparing schematics that contain MOSFETs.

FIGURE 5–35 The induced *p*-channel enhancement MOSFET



(a) Structure and electrical connections (b) Drain characteristics

FIGURE 5–36 Symbols for enhancement-type MOSFETs



I (a) *n*-channel (b) *p*-channel

II. (a) *n*-channel (b) *p*-channel

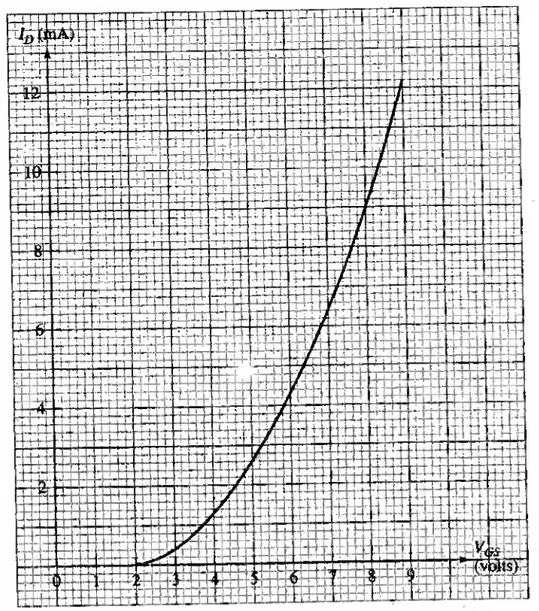


FIGURE 5-37 Transfer characteristic for an enhancement NMOS FET. $\beta = 0.5 \times 10^{-3}$; $V_T = 2$ V

Enhancement MOSFET Transfer Characteristic

In the active region, the drain current and gate-to-source voltage are related by

$$I_D = 0.5\beta(V_{GS} - V_T)^2 \qquad V_{GS} \geq V_T \tag{5-12}$$

where β is a constant whose value depends on the geometry of the device, among other factors. A typical value of β is 0.5×10^{-3} A/V^2. Figure 5–37 shows a plot of the transfer characteristic of an *n*-channel enhancement MOSFET for which $\beta = 0.5 \times 10^{-3}$ A/V^2 and $V_T = 2$ V.

Enhancement MOSFET Bias Circuits

Enhancement MOSFETs are widely used in digital integrated circuits (and require no bias circuitry in those applications). They also find applications in discrete- and integrated-circuit small-signal amplifiers. Figure 5–38, shows one way to bias a discrete enhancement NMOS for such an application. The resistor R_S does not provide self-bias as it does in the JFET circuit. Self-bias is not possible with enhancement devices. In Figure 5–38 the resistor R_S is used to provide feedback for bias stabilization, in the same way that the emitter resistor does in a BJT bias circuit. The larger the value of R_S, the less sensitive the bias point is to changes in MOSFET parameters caused by temperature changes or by device replacement. Recall that R_S in a JFET self-bias circuit also provides this beneficial effect.

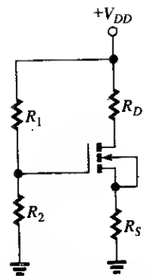
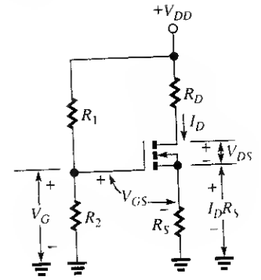


FIGURE 5–38 A bias circuit for an enhancement MOSFET

Figure 5–39 shows the voltage drops in the enhancement MOSFET bias circuit. R_1 and R_2 form a voltage divider that determines the gate-to-ground voltage V_G:

FIGURE 5–39 Voltage drops in the enhancement NMOS bias circuit



$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} \tag{5-13}$$

The voltage divider is not loaded by the very large input resistance of the MOSFET, so the values of R_1 and R_2 are usually made very large to keep the ac input resistance of the stage large. Writing Kirchhoff's voltage law around the gate-to-source loop, we find

$$V_{GS} = V_G - I_D R_S \qquad \text{(NMOS)} \tag{5-14}$$

For a PMOS device, V_G and V_{GS} are negative, so equation 5–14 would be written

$$V_{GS} = V_G + I_D R_S \qquad \text{(PMOS)} \tag{5-15}$$

(Note that I_D is considered positive in both equations.) Writing Kirchhoff's voltage law around the drain-to-source loop, we find

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \qquad \text{(NMOS)} \tag{5-16}$$

Again regarding I_D as positive in both the NMOS and PMOS devices, the counterpart of equation 5–16 for a PMOS device is

$$V_{DS} = -|V_{DD}| + I_D(R_D + R_S) \qquad \text{(PMOS)} \tag{5-17}$$

V_{DS} is negative in a PMOS circuit; note that the absolute value of V_{DD} must be used in equation 5–17 to obtain the correct sign for V_{DS}.

Equation 5–14 can be rewritten in the form

$$I_D = -(1/R_S)V_{GS} + V_G/R_S \tag{5-18}$$

Equation 5–18 is seen to be the equation of a straight line on the $I_D - V_{GS}$-axes. It intercepts the I_D-axis at V_G/R_S and the V_{GS}-axis at V_G. The line can be plotted on the same set of axes as the transfer characteristics of the device, and the point of intersection locates the bias values of I_D and V_{GS}.

General Algebraic Solution

We can obtain general algebraic expressions for the bias points in PMOS and NMOS circuits by solving equation 5–12 simultaneously with equation 5–14 or 5–15 for I_D. The results are shown as equation 5–19 and are valid for both NMOS and PMOS devices.

General algebraic solution for the bias point of NMOS and PMOS circuits

$$|V_G| = \frac{R_2}{R_1 + R_2}|V_{DD}|$$

$$I_D = \frac{-B \mp \sqrt{B^2 - 4AC}}{2A}$$

where $A = R_S^2$

$$B = -2\left((|V_G| - |V_t|)R_S + \frac{1}{\beta}\right)$$

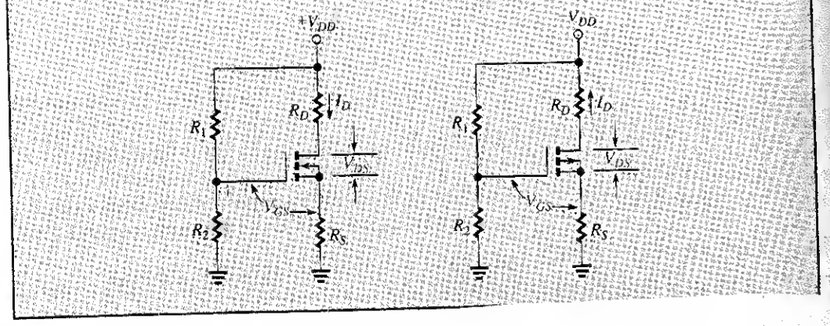
$C = (|V_G| - |V_t|)^2$

$|V_{DS}| = |V_{DD}| - I_D(R_D + R_S)$ See note 1.

$|V_{GS}| = |V_G| - I_D R_S$ See note 2.

Note 1. V_{DS} is positive for an NMOS FET and negative for a PMOS FET.

Note 2. V_{GS} is positive for an NMOS FET and negative for a PMOS FET.



EXAMPLE 5–9

The transfer characteristic of the NMOS FET in Figure 5–40 is given in Figure 5–41 ($\beta = 0.5 \times 10^{-3}$ and $V_T = 2$ V). Determine values of V_{GS}, I_D, and V_{DS} at the bias point (1) graphically and (2) algebraically.

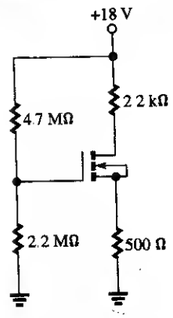


FIGURE 5–40
(Example 5–9).

Solution

1. From equation 5–13,

$$V_G = \left(\frac{22 \times 10^6}{47 \times 10^6 + 22 \times 10^6}\right) 18 \text{ V} = 5.74 \text{ V}$$

Substituting in equation 5–18, we have

$$I_D = -2 \times 10^{-3} V_{GS} + 11.48 \times 10^{-3}$$

This equation intersects the I_D-axis at 11.48 mA and the V_{GS}-axis at $V_G = 5.74$ V. It is shown plotted with the transfer characteristic in Figure 5–41. The two plots intersect at the quiescent point, where the values of I_D and V_{GS} are approximately $I_D = 2.0$ mA and $V_{GS} = 4.6$ V. The corresponding quiescent value of V_{DS} is found from equation 5–16:

$$V_{DS} = 18 - (2.0 \text{ mA})[(2.2 \text{ k}\Omega) + (0.5 \text{ k}\Omega)] = 12.60 \text{ V}$$

In order for this analysis to be valid, the Q-point must be in the saturation region: that is, we must have $V_{DS} > V_{GS} - V_T$. In our example, we have

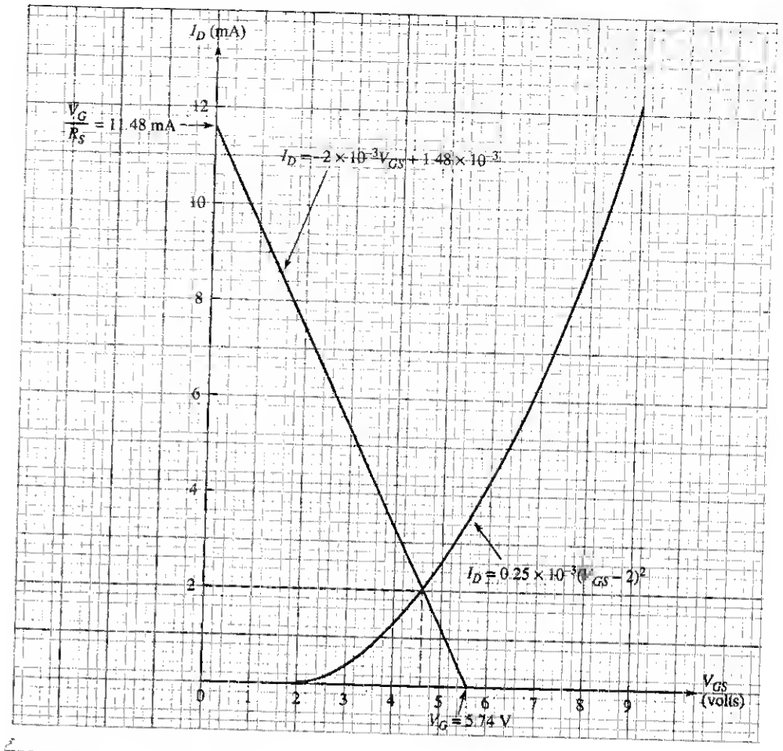


FIGURE 5–41 (Example 5–9)

$V_{DS} = 12.60$ V and $V_{GS} - V_T = 2.6$ V, so we know the results are valid. The validity criterion can be expressed for both NMOS and PMOS FETs as $|V_{DS}| > |V_{GS} - V_T|$.

2. We have already found $V_G = 5.74$ V. Using $R_S = 500\ \Omega$, $R_D = 2.2$ kΩ, $V_{DD} = 18$ V, $V_T = 2$ V, and $\beta = 0.5 \times 10^{-3}$, we have, with reference to equations 5–19

$$A = (500)^2 = 2.5 \times 10^5$$
$$B = -2[(5.74 - 2)500 + 1/(0.5 \times 10^{-3})] = -7.74 \times 10^3$$
$$C = (5.74 - 2)^2 = 13.9876$$

Substituting these values into the equation for I_D, we find $I_D = 1.927$ mA. Then, $V_{DS} = 18 \text{ V} - (1.927 \text{ mA})(2.2 \text{ k}\Omega + 500\ \Omega) = 12.8$ V and $V_{GS} = 5.74 \text{ V} - (1.927 \text{ mA})(500\ \Omega) = 4.78$ V. These results agree well with those obtained graphically in part 1.

EXAMPLE 5–10

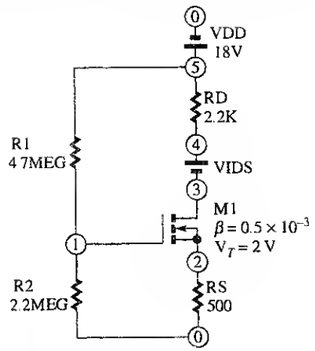
SPICE

Use SPICE to find I_D, V_{DS} and V_{GS} for the figure shown.

Solution

The SPICE circuit and input data file are shown in Figure 5–42(a). Note that the parameter V_T is entered in the .MODEL statement as VTO = 2 and that β is entered as KP = 0.5E−3 (see Section A–12). All other parameter values are

FIGURE 5–42 (Example 5–10)



(a)

```
EXAMPLE 5-10
M1 3 1 2 2 MOSFET
.MODEL MOSFET NMOS VTO=2 KP=0.5E-3
R1 5 1 4.7MEG
R2 1 0 2.2MEG
RS 2 0 500
VIDS 4 3
RD 5 4 2.2K
VDD 5 0 18V
.END
```

```
EXAMPLE 5-10
****     DC TRANSFER CURVES              TEMPERATURE = 27.000 DEG C
******************************************************************************
   VDD          I(VIDS)        V(3,2)         V(1,2)
1.800E+01     1.926E-03     1.280E+01     4.776E+00
```

(b)

allowed to default. The results of the analysis are shown in Figure 5–42(**b**). We see that I_D = I(VIDS) = 1.926 mA, V_{DS} = V(3, 2) = 12.8 V and V_{GS} = V(**1, 2**) = 4.776 V, in good agreement with the previous example.

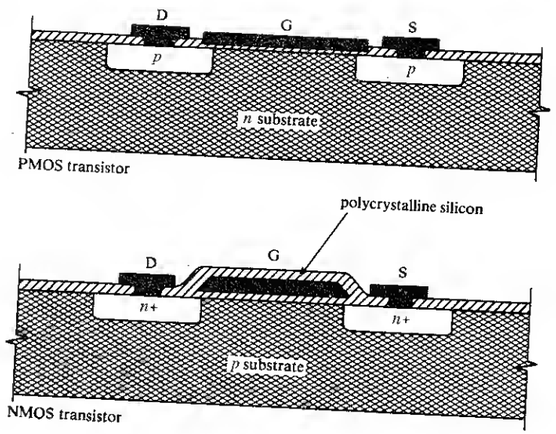
5–8 INTEGRATED-CIRCUIT MOSFETS

By far the greatest number of MOSFETs manufactured today are in integrated circuits. The enhancement-type MOSFET has a very simple structure (Figure 5–31) that makes its fabrication in a crystal substrate a straightforward and economical procedure. Furthermore, a very great number of devices can be fabricated in a single chip. Enhancement MOSFETs account for the vast majority of very large scale integrated (VLSI) circuits manufactured, and they are the primary ingredients of digital ICs such as microprocessors and computer memories.

The fabrication of integrated-circuit MOSFETs is accomplished using photolithographic techniques and batch production methods. Because millions of components may be fabricated in a single VLSI chip, the techniques we described for producing very fine masks and for direct writing of patterns using electron beams are particularly appropriate to VLSI technology. Ion implantation, which allows close control of impurity concentration and layer depth, is widely used to control the values of threshold voltages and other MOSFET characteristics.

Figure 5–43 shows cross-sectional views of PMOS and NMOS FETs embedded in crystal substrates. Note that a layer of polycrystalline silicon is deposited over the gate of an NMOS device to form the gate terminal. This layer improves device performance but adds to the complexity of the manufacturing procedure. PMOS devices are less expensive to produce but do not perform as well as NMOS circuits, primarily because the mobility of the majority carriers (holes) in *p* material is smaller than that of the majority carriers (electrons) in *n* material. NMOS circuits are generally preferred and can be produced with the greatest number of components per chip for a given performance capability.

FIGURE 5–43 Cross-sectional views of integrated-circuit MOSFETs



Another type of digital integrated circuit using enhancement MOSFETs has both PMOS and NMOS devices embedded in the same substrate. These circuits are called *complementary* MOS, or CMOS, circuits. They are more difficult to construct than either PMOS or NMOS circuits, but they have the best performance characteristics, especially in terms of switching speed. We will discuss applications of CMOS circuitry in Chapter 18. Figure 5–44 shows a cross-sectional view of a CMOS circuit containing one PMOS and one NMOS transistor. Note that it is necessary to embed a *p*-type layer in the *n* substrate for the NMOS transistor. This *p* layer, frequently called a "tub" or "*p*-well," is necessary for the formation of the *induced n* channel of the NMOS transistor. Also note the n^+ and p^+ regions used to isolate the transistors. The CMOS structure is made with a polycrystalline silicon gate electrode. The more complex structure of a CMOS IC is evident in the figure.

5–9 VMOS AND DMOS TRANSISTORS

VMOS Transistors

Still another variation in MOS structure is called VMOS, which is used to produce both *n*-channel and *p*-channel enhancement MOSFETs. The name is derived from the appearance of the cross-sectional view (Figure 5–45), in which it can be seen that a V-shaped groove penetrates alternate *n* and *p* layers. (In reality, the device is formed in a crater shaped like an inverted pyramid.) As can be seen in the *n*-channel VMOS transistor shown in Figure 5–45, the length of the induced *n* channel is determined by the *thickness* of the *p* layer. The layers

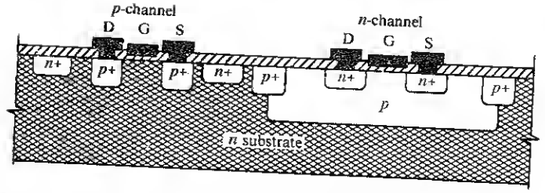


FIGURE 5–44 Complementary MOS (CMOS) integrated circuit containing both NMOS and PMOS devices

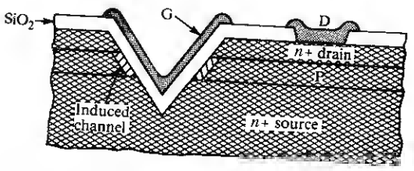


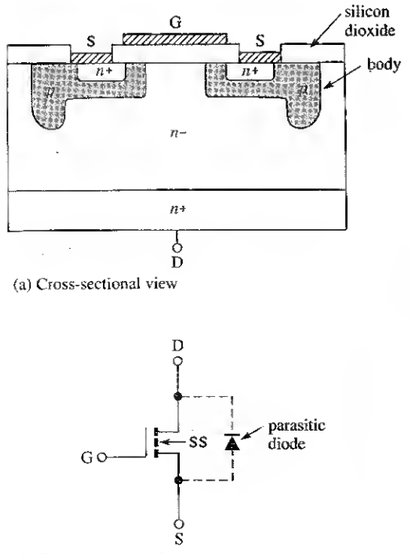
FIGURE 5–45 VMOS structure. Note that the length of the channel depends on the thickness of the diffused *p* layer.

are formed using epitaxial growth and diffusion methods, which provide good control over thickness and therefore good control of channel length. Since the aspect ratio of the channel determines some important properties of the FET, this control is a valuable feature of the method. Also, the technique conserves space on the chip surface because the channel can be made longer simply by making the *p* region thicker. As a result, a greater number of devices can be created in one chip using conventional photolithographic methods. Finally, VMOS transistors have greater current-handling capabilities than their planar counterparts and are finding use in power-amplifier applications.

DMOS Transistors

DMOS is an FET structure created specifically for high-power applications. It is a planar transistor whose name is derived from the double-diffusion process used to construct it. Figure 5–46(a) shows a cross-sectional view. Note that drain-to-source current flows through a *p*-type channel region (that is inverted by a positive gate-to-source voltage), an n^- (lightly doped) epitaxial region, and n^+ substrate. The channel length can be closely controlled in the diffusion process and is typically very short (a few micrometers). For this reason, it is called a *short-channel* MOS transistor. DMOS transistors are widely used for *switching* heavy currents and high voltages and switching regulators.

The DMOS transistor has a *parasitic* diode between its drain and source. A parasitic component of a semiconductor device is one that exists as a result of the structure of the device rather than by design. In other words, the parasitic diode in a DMOS transistor is inherent in its structure of *p* and *n* layers: Its existence is inevitable. In Figure 5–46(a), the n^+ source and the *p* channel (called the *body*) form an *electrical bond* rather than a *pn* junction. The parasitic diode is the *pn* junction between the body and drain. Because the body is electrically connected to the source, the parasitic diode is effectively connected across the drain and source terminals, with the anode connected to



(a) Cross-sectional view

(b) Schematic symbol

FIGURE 5–46 The DMOS transistor

source and the cathode connected to drain. The schematic symbol for the DMOS transistor often includes the parasitic diode, as shown in Figure 5–46(b).

One property shared by short-channel power FETs is that they have a *linear* transfer characteristic. That is, when the gate-to-source voltage is greater than the threshold voltage, the drain current is a linear function of the gate-to-source voltage rather than the nonlinear function illustrated in Figure 5–37. The linear transfer characteristic of short-channel devices is the result of a phenomenon called *velocity saturation*, whereby the velocity of charge carriers reaches but does not exceed a certain value as drain-to-source current increases.

5–10 FET CIRCUIT ANALYSIS WITH ELECTRONICS WORKBENCH MULTISIM

This section examines the use of EWB to simulate a JFET transistor switch. The JFET can be used as an analog switch as described in Section 5–5. To begin the exercise, open the file Ch5-EWB.msm that is found in the Electronics Workbench Multisim 2001 CD-ROM packaged with the text. The circuit being demonstrated is shown in Figure 5–47. This is a JFEI chopper circuit. Q1 is an ideal JFET transistor being driven by the function generator (XFG1). The resistor R1 is simulating the load, the input signal is a 2 $V_{p\text{-}p}$ 1000 Hz signal. The EWB oscilloscopes have been connected to monitor the input signal (XSC2), the function generator input signal, and the circuit output (XSC1).

This application will demonstrate the operation of a JFEI chopper. The JFET transistor will be set up to switch from the cutoff region ($V_{GS} = V_P = -2$ V) to the pinch-off region ($V_{GS} = 0$). The EWB Multisim ideal transistor will be used. The model parameters for the JFEI transistor can be viewed by double-clicking on the JFEI. This opens the menu shown in Figure 5–48.

Click on Edit Model to view the model parameters used by EWB Multisim. This opens the list shown in Figure 5–49. Notice that VTO = −2. This is the setting for the pinch-off voltage for the transistor.

Double-click on the function generator (XFG1) to set the signal levels to those shown in Figure 5–50. The function generator is set to produce a square-wave with a sample frequency of 50 Hz. The offset voltage is set to −2 V and the amplitude is 2 V. The function generator will produce a square-wave that

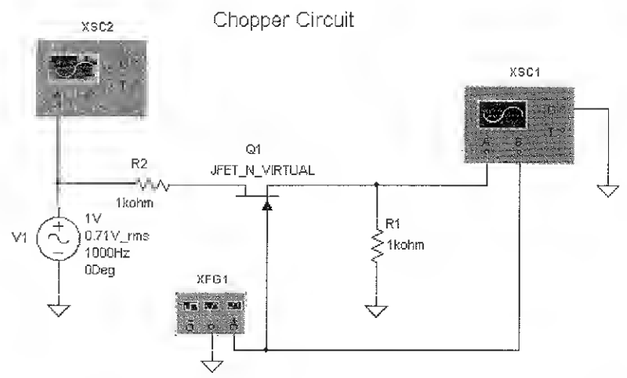
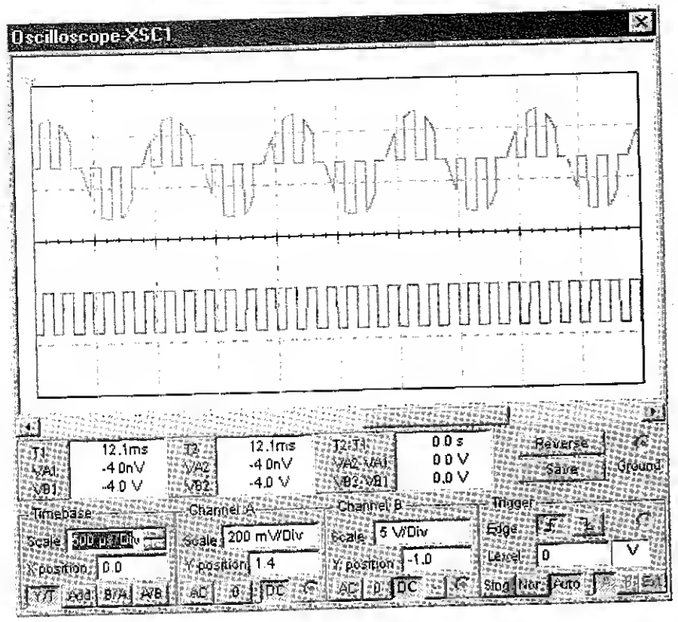


FIGURE 5–47 The JFEI chopper circuit used in the EWB exercise

FIGURE 5–52 The output of the JFET chopper



SUMMARY

This chapter has presented the basics of the FET transistor. Students should have mastered these concepts and skills:

- Basic circuit analysis techniques.
- JFET transistor circuit analysis to identify the cutoff, pinch-off, and voltage-controlled–resistance of operation.
- Using the JFET transistor as an analog switch
- How to bias a discrete MOSFET transistor.

EXERCISES

SECTION 5–2

Junction Field-Effect Transistors

5–1. An *n*-channel JFET has the drain characteristics shown in Figure 5–6. Find the approximate dc resistance between drain and source when $V_{DS} = 1$ V and (a) $V_{GS} = 0$ V, (b) $V_{GS} = -1$ V, and (c) $V_{GS} = -2$ V. Explain why these results confirm that these points lie in the voltage-controlled–resistance region of the characteristics

5–2. An *n*-channel JFET has $I_{DSS} = 16$ mA and $V_p = -6$ V.

(a) What is the value of $V_{DS(sat)}$ when $V_{GS} = -4$ V?

(b) What is the saturation current at $V_{GS} = -4$ V?

5–3. A *p*-channel JFET has a pinch-off voltage of 8 V. At what value of V_{GS} does $V_{DS(sat)} = -3$ V?

5–4. Using the transfer characteristic shown in Figure 5–10, find approximate values for (a) I_D when $V_{DS} = 8$ V and $V_{GS} = -1.6$ V, and (b) V_{GS} when $V_{DS} = 8$ V and $I_D = 10$ mA.

5–5. Using the transfer characteristic shown in Figure 5–10, find the total change in I_D (ΔI_D) when (a) V_{GS} changes from -2.8 V to -1.8 V and (b) V_{GS} changes from -1.8 V to -0.8 V. What do these results tell you about the linearity of the device?

5–6. An *n*-channel JFET has a pinch-off voltage of -5.8 V and $I_{DSS} = 15$ mA. Assuming that it is operated in its pinch-off region, find the value of I_D when (a) $V_{GS} = 0$ V, (b) $V_{GS} = -2$ V, and (c) $V_{GS} = -6.5$ V.

5–7. An *n*-channel JFET having a pinch-off voltage of -3.5 V has a saturation current of 2.3 mA when $V_{GS} = -1$ V. What is its saturation current when (a) $V_{GS} = 0$ V and (b) $V_{GS} = -2$ V?

5–8. A *p*-channel JFET has a pinch-off voltage of 6 V and $I_{DSS} = 18$ mA. At what value of V_{GS} in the pinch-off region will I_D equal 6 mA? What is the value of V_{DS} at the boundary of the pinch-off and voltage-controlled–resistance regions when $I_D = 6$ mA?

SECTION 5–3

JFET Biasing

5–9. The JFET in the circuit of Figure 5–53 has the drain characteristics shown in Figure 5–14. Find the quiescent values of I_D and V_{DS} when (a) $V_{GS} = -2$ V and (b) $V_{GS} = 0$ V. Which, if either, of the Q-points is in the pinch-off region?

5–10. Using Figure 5–14, determine the value of V_{GS} in Exercise 5–9 that would be required to obtain $V_{DS} = 8$ V.

5–11. The JFET shown in Figure 5–54 has $I_{DSS} = 14$ mA and $V_p = -5$ V. Algebraically determine the quiescent values of I_D and V_{DS} for (a) $V_{GS} = -3.6$ V, (b) $V_{GS} = -3$ V, and (c) $V_{GS} = -1.7$ V. In each case, check the validity of your results by verifying that the quiescent point is in the pinch-off region. Identify any cases that do not meet that criterion and for which the results are therefore not valid.

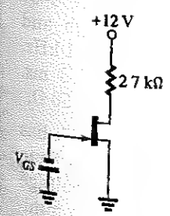


FIGURE 5–53 (Exercise 5–9)

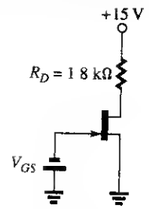


FIGURE 5–54 (Exercise 5–11)

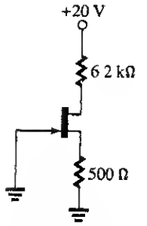


FIGURE 5–55 (Exercise 5–13)

5–12. Repeat Exercise 5–11 when R_D is changed to 1 kΩ. Does this modification affect the validity of the results in any of the three cases (a), (b), or (c)? Explain.

5–13. Figure 5–56 shows the transfer characteristics of the JFET in the circuit of Figure 5–55. Graphically determine the quiescent values of I_D and V_{GS}. Compute the quiescent value of V_{DS} based on your results and verify their validity.

5–14. Algebraically determine the quiescent values of I_D, V_{GS}, and V_{DS} in the circuit of Exercise 5–13. (Refer to Figure 5–56 to obtain values for I_{DSS} and V_p.)

5–15. Figure 5–58 shows the transfer characteristic for the JFET in the circuit of Figure 5–57.

(a) Graphically determine the quiescent values of I_D and V_{GS}. Compute the quiescent value of V_{DS} based on your results and verify their validity.

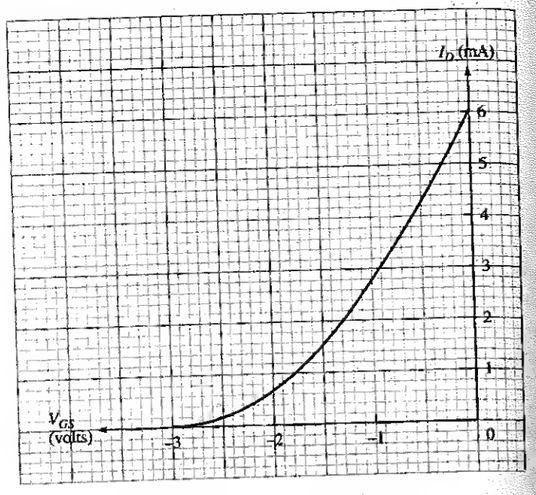
(b) Determine the quiescent values of I_D, V_{GS}, and V_{DS} algebraically.

SECTION 5–4

The JFET Current Source

5–16. The JFET shown in Figure 5–59 has $V_p = -5$ V and $I_{DSS} = 12$ mA. What is the

FIGURE 5–56 (Exercise 5–13)



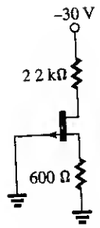
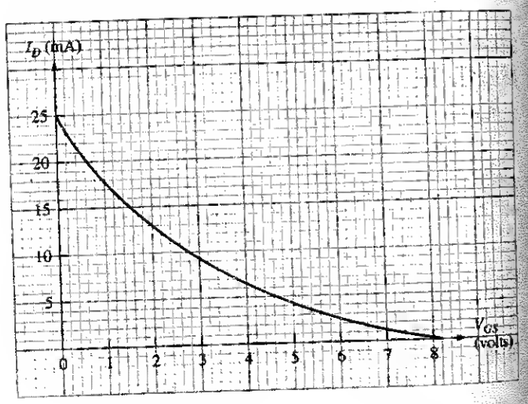


FIGURE 5–57 (Exercise 5–15)

FIGURE 5–58 (Exercise 5–15)



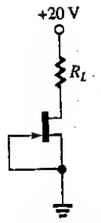


FIGURE 5–59
(Exercise 5–16)

maximum value of R_L for which the circuit can be used as a constant-current source?

5–17. When $V_{GS} = 0$ V, the JFET shown in Figure 5–60 begins to break down at $V_{DS} = 15$ V. If $V_p = -3.5$ V and $I_{DSS} = 10$ mA, over what range of R_L can the circuit be used as a constant-current source?

5–18. When $V_{GS} = 0$ V, the JFET shown in Figure 5–61 begins to break down at $V_{DS} = 18$ V. If $V_p = 4$ V and $I_{DSS} = 12$ mA, over what range of R_L can the circuit be used as a constant-current source?

SECTION 5–5

The JFET as an Analog Switch

5–19. The drain-to-source resistance when the JFET in Figure 5–62 is conducting is 80 Ω. If $v_d = 0.16$ V, find the load voltage v_L (a) when $V_{GS} = V_p$ and (b) when $V_{GS} = 0$ V.

5–20. The JFET in Figure 5–63 has $R_{D(ON)} = 100$ Ω and $V_p = 4$ V. If $v_i = 0.1 \sin 1000t$, write the expression for v_L (a) when $V_{GS} = 4$ V and (b) when $V_{GS} = 0$ V.

5–21. The square wave shown in Figure 5–64 turns the chopper ON when high and OFF when low. If it has frequency 1 kHz, sketch v_L over a time period of 3 ms. Assume that $R_{D(ON)}$ for the JFET is 50 Ω.

5–22. The JFET shown in Figure 5–65 has $R_{D(ON)} = 40$ Ω. If the output voltage is to be no less than 90% of the signal voltage when the JFET is ON, what is the minimum permissible value of R_L?

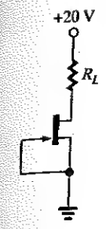


FIGURE 5–60 (Exercise 5–17)

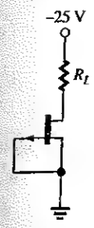


FIGURE 5–61 (Exercise 5–18)

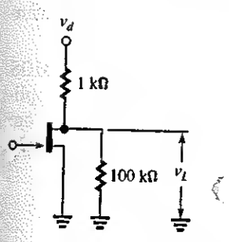


FIGURE 5–62 (Exercise 5–19)

SECTION 5–6

Manufacturers' Data Sheets

5–23. By referring to the manufacturer's data sheets for the 2N4220–2N4222 series of JFETs and assuming that $T = 25$°C, determine the following:

(a) What is the maximum permissible drain current in each device?

(b) What is the maximum pinch-off voltage for 2N4221 transistors?

(c) What is the maximum permissible value of V_{GS} for each device?

(d) For which device is the variation in possible values of I_{DSS} the greatest (in terms of the ratio of maximum to minimum values)?

5–24. Refer to the manufacturer's data sheet in Figure 5–30 to determine the following:

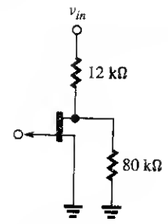


FIGURE 5–63 (Exercise 5–20)

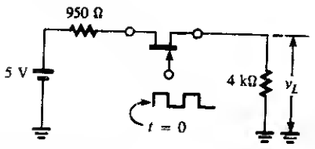


FIGURE 5–64 (Exercise 5–21)

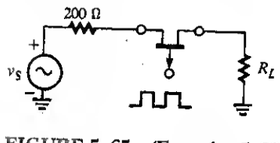


FIGURE 5–65 (Exercise 5–22)

(a) Locate the transfer characteristic that shows the maximum value of I_{DSS} to be 12 mA at 40°C. What is the approximate value of V_{GS} at the point of zero temperature coefficient? What is the approximate maximum value of I_{DSS} at 25°C?

(b) Locate the drain characteristics for which I_{DSS} is approximately 1.4 mA. What is the approximate dc resistance between drain and source when $V_{DS} = 0.5$ V and $V_{GS} = 0$ V? At what value of V_{DS} will $I_D = 1.2$ mA when $V_{GS} = -0.1$ V?

SECTION 5–7

Metal-Oxide-Semiconductor FETs

5–25. An induced *n*-channel enhancement MOSFET has the drain characteristics shown in Figure 5–34. At what value of V_{DS} would a curve corresponding to $V_{GS} = 7.35$ V intersect the parabola?

5–26. The induced *n*-channel enhancement MOSFET whose drain characteristics are shown in Figure 5–34 is to be operated in its active region with a drain

current of 10.4 mA. What value should V_{DS} exceed?

5–27. An enhancement NMOS FET has $\beta = 0.5 \times 10^{-3}$ and $V_T = 2.5$ V. Find the value of I_D when (a) $V_{GS} = 6.14$ V, and (b) $V_{GS} = 0$ V.

5–28. An enhancement PMOS FET has $\beta = 0.5 \times 10^{-3}$ and $V_T = -2$ V. What is the value of V_{GS} when $I_D = 10.32$ mA?

5–29. An enhancement NMOS FET has the transfer characteristic shown in Figure 5–37.

(a) Graphically determine V_{GS} when $I_D = 6.4$ mA.

(b) Algebraically determine V_{GS} when $I_D = 6.4$ mA.

5–30. In the bias circuit of Figure 5–30, $R_1 = 2.2$ mΩ, $R_2 = 1$ mΩ, $V_{DD} = 28$ V, $R_D = 2.7$ kΩ, and $R_s = 600$ Ω. If $V_{GS} = 5.5$ V, find (a) I_D and (b) V_{DS}.

5–31. In the bias circuit of Figure 5-38, $R_1 = 470$ kΩ, $V_{DD} = 20$ V, $R_D = 1.5$ kΩ, $R_s = 220$ Ω, $I_D = 6$ mA, and $V_{GS} = 6$ V. Find (a) V_{DS} and (b) R_2.

5–32. The MOSFET in Figure 5–66 has $\beta = 0.62 \times 10^{-3}$ and $V_T = -2.4$ V. Algebraically determine the quiescent values of I_D, V_{GS}, and V_{DS}. Verify the validity of your results

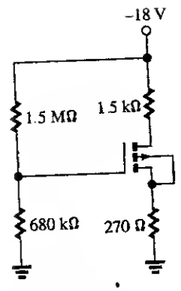


FIGURE 5–66 Exercise 5–32

SECTION 5–8

Integrated-Circuit MOSFETs

5–33. What does CMOS stand for? Why is it so named?

SECTION 5–9

VMOS and DMOS Transistors

5–34. List and briefly describe three advantages of VMOS technology.

5–35. What process is used to construct DMOS transistors? What is their primary application? What characteristics make them different from conventional MOSFETs?

SPICE EXERCISES

5–36. Verify the answers to Example 5–3 using SPICE analysis. BETA = .62SE−3, VTO = −4 for $V_{GS} = -1.5$ V. Why do the answers in Example 5–3 differ from the SPICE results?

5–37. Use SPICE to simulate the JFET chopper circuit shown in Figure 5–28. Use a 1–V p-p 1-kHz sinusoid for the input, a source resistance of 600 Ω, and a gate pulse of 0 to −5 V with a pulse width of 100 μs and a period of 200 μs. The BETA of the transistor is 7.5 E−4 and VTO = −4.

```
VS 5 0 SIN(0 5 1kHz)
RS 5 2 600
VG 3 0 PULSE(0 -5 0 1µs 1µs 100µs 200µs)
.MODEL NFET NJF BETA = 7.5E-4 VTO=-4
```

Provide a plot of the input sinusoid, the gate pulse, and the output waveform. What is the output waveform called?

CHAPTER 6

AMPLIFIER FUNDAMENTALS

OUTLINE